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50	BOM

IB15A-AHS VER 6.0

CPU:
Intel Skylake S 42 in LGA1151 Package 95W

System Chipset:
SPT-H PCH

Main Memory:
Dual Channel/DDR4+DDR3 (Max 16GB) 1066/1333/1600

Onboard Device:
Super I/O:IT8625E
LAN:INTEL I219
HD Codec:ALC892
PCI BRIDGE ASM1083

Power solution:
CPU Voltage Regulators:3phase by ISL95856+ISL95857
DDR Voltage Regulators:1Phase by UP1514

Expansion Slots:
PCI EXPRESS 16X SLOT *1
PCI EXPRESS 1X SLOT *1
PCI SLOT *3
PCI EXPRESS 16X(4 LANES) SLOT *1

REAR IO:
PS/2 +2 layer USB2.0 Port
HDMI Port
DVI+VGA Port
USB3.0 PORT *2
Gb RJ-45 +2 layer USB3.0 Ports
Audio Jackets (6 PORT)

Front I/O:
SATA3 *4
SATA EXPRESS * 1
USB 2.0 Header * 2
USB 3.0 Header * 2
CPU FAN *1
System FAN *2
Serial header
CIR Header
Front Audio Header

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BIOSTAR GROUP

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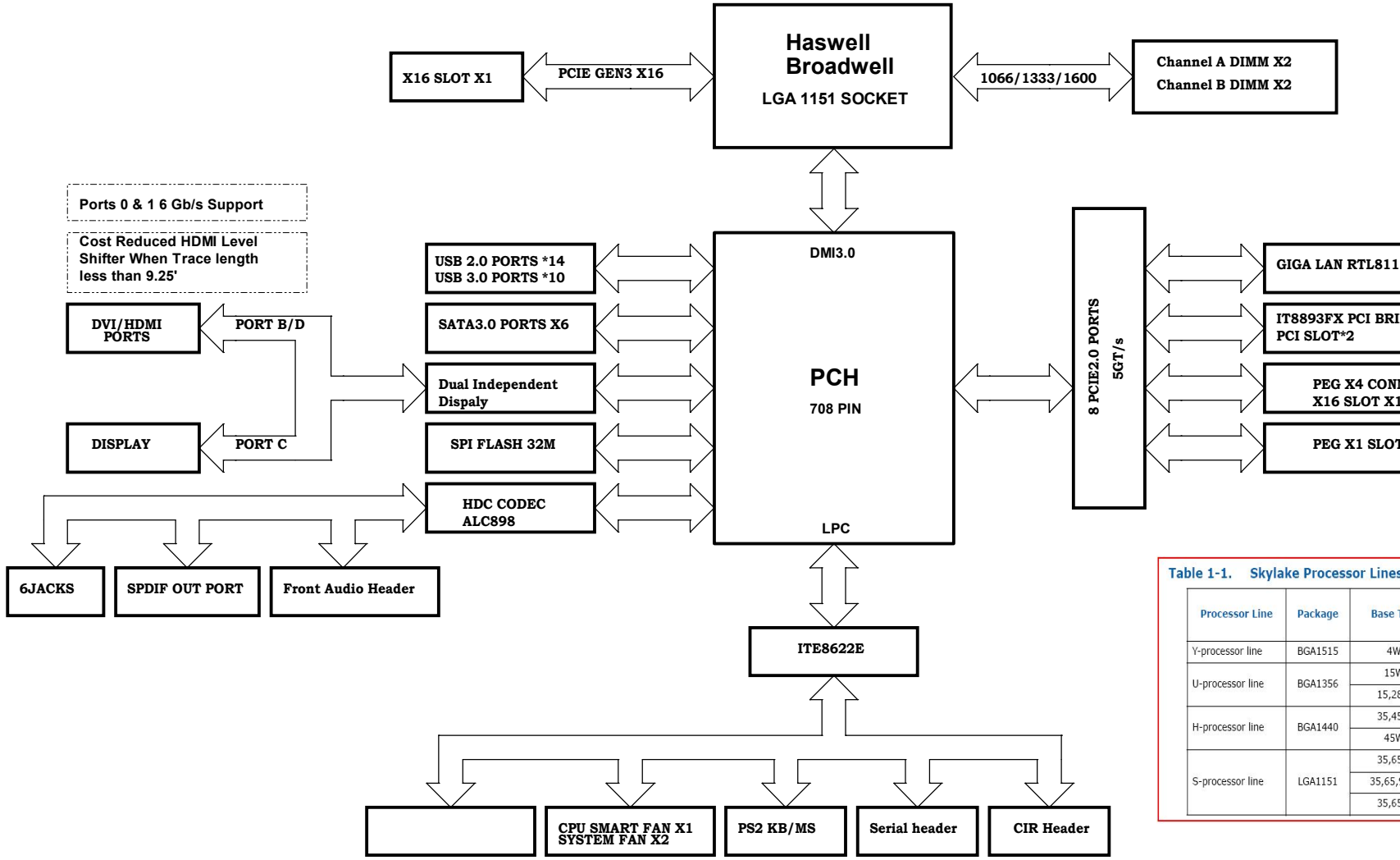

Table 1-1. Skylake Processor Lines

Processor Line	Package	Base TDP	Processor IA Cores	Maximum Graphics Configuration	On Package Cache	Platform Type
Y-processor line	BGA1515	4W	2	GT2	N/A	1-Chip
U-processor line	BGA1356	15W	2	GT2		1-Chip
		15,28W		GT3	64 MB	
H-processor line	BGA1440	35,45W	4	GT2	N/A	2-Chip
		45W	4	GT4	128 MB	
S-processor line	LGA1151	35,65W	2	GT2	N/A	2-Chip
		35,65,95W	4	GT2		
		35,65W	4	GT4	64 MB	

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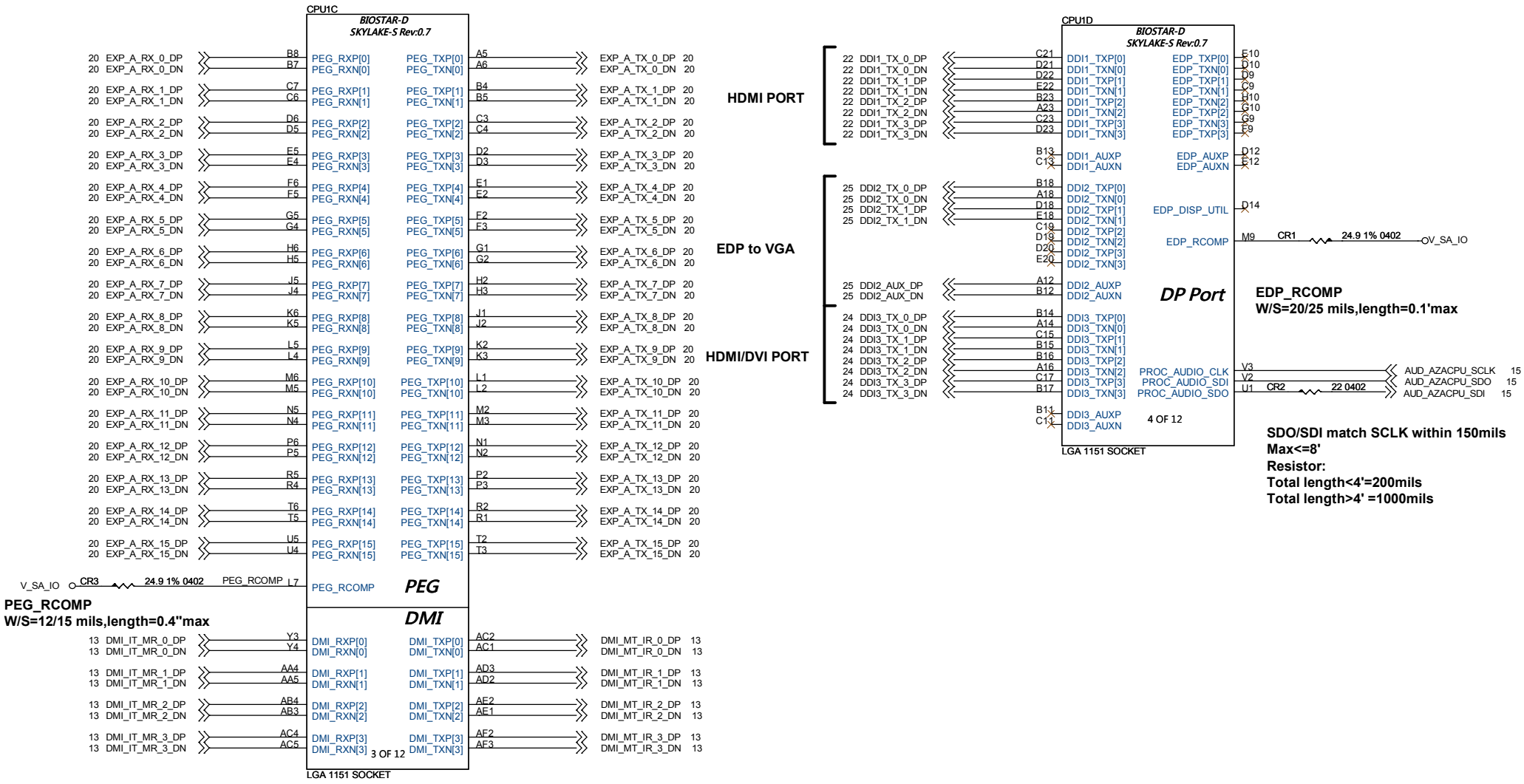

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Title	CPU PCIEX16/DMI/FDI		
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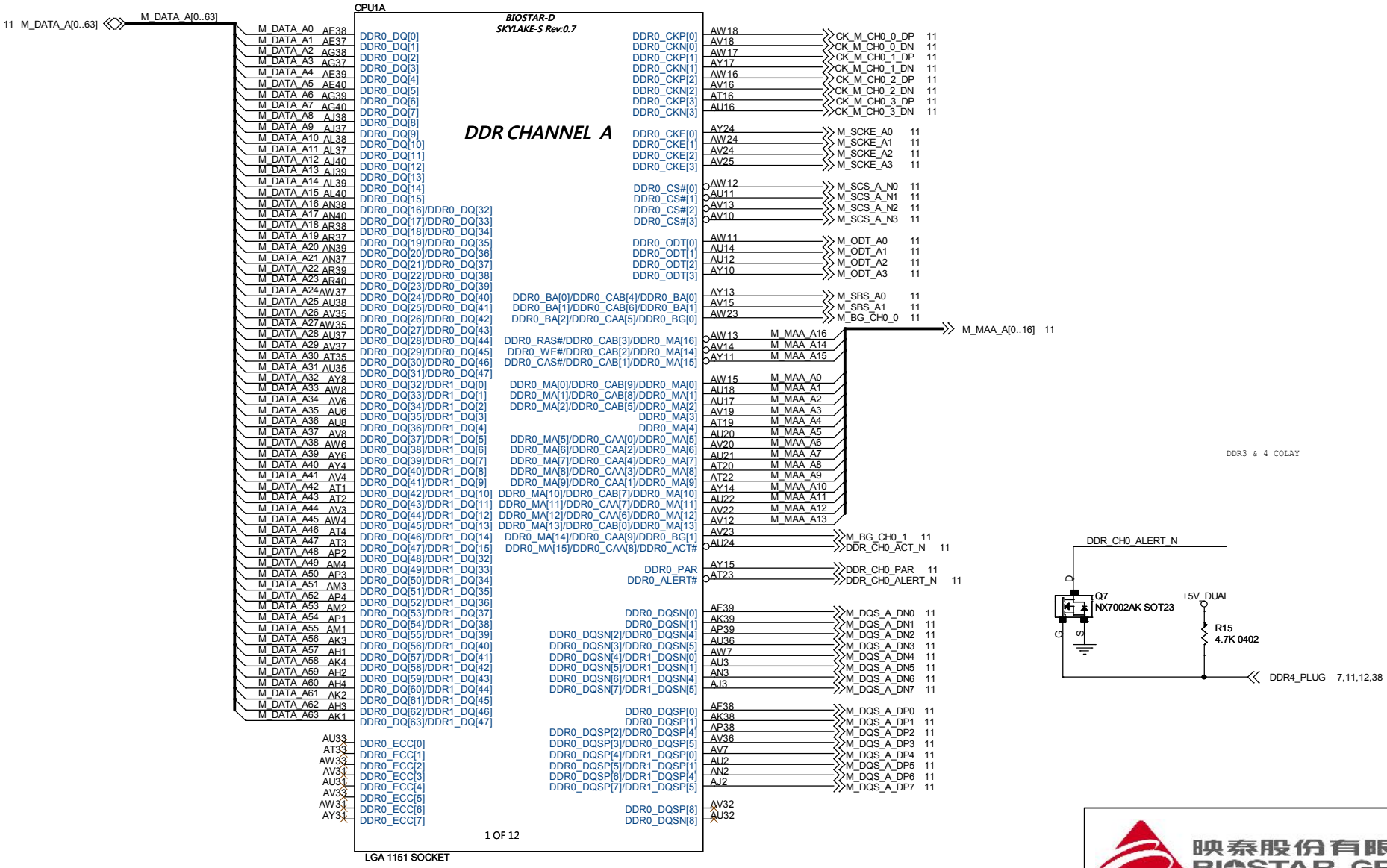

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Title	CPU DDR4 CHANNEL A	
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CPU1B

BIOSTAR-D
SKYLAKE-S
Rev:0.7

DDR CHANNEL B

12 M_DATA_B[0..63] → M_DATA_B[0..63]

M_DATA_B0	AD34	DDR1_DQ[0]/DDR0_DQ[16]	
M_DATA_B1	AD35	DDR1_DQ[1]/DDR0_DQ[17]	
M_DATA_B2	AG35	DDR1_DQ[2]/DDR0_DQ[18]	
M_DATA_B3	AH35	DDR1_DQ[3]/DDR0_DQ[19]	
M_DATA_B4	AE35	DDR1_DQ[4]/DDR0_DQ[20]	
M_DATA_B5	AE34	DDR1_DQ[5]/DDR0_DQ[21]	
M_DATA_B6	AG34	DDR1_DQ[6]/DDR0_DQ[22]	
M_DATA_B7	AH34	DDR1_DQ[7]/DDR0_DQ[23]	
M_DATA_B8	AK35	DDR1_DQ[8]/DDR0_DQ[24]	
M_DATA_B9	AL35	DDR1_DQ[9]/DDR0_DQ[25]	
M_DATA_B10	AK32	DDR1_DQ[10]/DDR0_DQ[26]	
M_DATA_B11	AL32	DDR1_DQ[11]/DDR0_DQ[27]	
M_DATA_B12	AK34	DDR1_DQ[12]/DDR0_DQ[28]	
M_DATA_B13	AL34	DDR1_DQ[13]/DDR0_DQ[29]	
M_DATA_B14	AK31	DDR1_DQ[14]/DDR0_DQ[30]	
M_DATA_B15	AL31	DDR1_DQ[15]/DDR0_DQ[31]	
M_DATA_B16	AP35	DDR1_DQ[16]/DDR0_DQ[48]	
M_DATA_B17	AN35	DDR1_DQ[17]/DDR0_DQ[49]	
M_DATA_B18	AN32	DDR1_DQ[18]/DDR0_DQ[50]	
M_DATA_B19	AP32	DDR1_DQ[19]/DDR0_DQ[51]	
M_DATA_B20	AN34	DDR1_DQ[20]/DDR0_DQ[52]	
M_DATA_B21	AP34	DDR1_DQ[21]/DDR0_DQ[53]	
M_DATA_B22	AN31	DDR1_DQ[22]/DDR0_DQ[54]	
M_DATA_B23	AP31	DDR1_DQ[23]/DDR0_DQ[55]	
M_DATA_B24	AL29	DDR1_DQ[24]/DDR0_DQ[56]	
M_DATA_B25	AM29	DDR1_DQ[25]/DDR0_DQ[57]	
M_DATA_B26	AP29	DDR1_DQ[26]/DDR0_DQ[58]	
M_DATA_B27	AR29	DDR1_DQ[27]/DDR0_DQ[59]	
M_DATA_B28	AM28	DDR1_DQ[28]/DDR0_DQ[60]	
M_DATA_B29	AL28	DDR1_DQ[29]/DDR0_DQ[61]	
M_DATA_B30	AR28	DDR1_DQ[30]/DDR0_DQ[62]	
M_DATA_B31	AP28	DDR1_DQ[31]/DDR0_DQ[63]	
M_DATA_B32	AR12	DDR1_DQ[32]/DDR1_DQ[16]	
M_DATA_B33	AP12	DDR1_DQ[33]/DDR1_DQ[17]	
M_DATA_B34	AM13	DDR1_DQ[34]/DDR1_DQ[18]	
M_DATA_B35	AL13	DDR1_DQ[35]/DDR1_DQ[19]	
M_DATA_B36	AR13	DDR1_DQ[36]/DDR1_DQ[20]	
M_DATA_B37	AP13	DDR1_DQ[37]/DDR1_DQ[21]	
M_DATA_B38	AM12	DDR1_DQ[38]/DDR1_DQ[22]	
M_DATA_B39	AL12	DDR1_DQ[39]/DDR1_DQ[23]	
M_DATA_B40	AP10	DDR1_DQ[40]/DDR1_DQ[24]	
M_DATA_B41	AR10	DDR1_DQ[41]/DDR1_DQ[25]	
M_DATA_B42	AR7	DDR1_DQ[42]/DDR1_DQ[26]	
M_DATA_B43	AP7	DDR1_DQ[43]/DDR1_DQ[27]	
M_DATA_B44	AR9	DDR1_DQ[44]/DDR1_DQ[28]	
M_DATA_B45	AP9	DDR1_DQ[45]/DDR1_DQ[29]	
M_DATA_B46	AR6	DDR1_DQ[46]/DDR1_DQ[30]	
M_DATA_B47	AP6	DDR1_DQ[47]/DDR1_DQ[31]	
M_DATA_B48	AM10	DDR1_DQ[48]	
M_DATA_B49	AL10	DDR1_DQ[49]	
M_DATA_B50	AM7	DDR1_DQ[50]	
M_DATA_B51	AL7	DDR1_DQ[51]	
M_DATA_B52	AM9	DDR1_DQ[52]	
M_DATA_B53	AL9	DDR1_DQ[53]	
M_DATA_B54	AM6	DDR1_DQ[54]	
M_DATA_B55	AL6	DDR1_DQ[55]	
M_DATA_B56	AJ6	DDR1_DQ[56]	
M_DATA_B57	AJ7	DDR1_DQ[57]	
M_DATA_B58	AE6	DDR1_DQ[58]	
M_DATA_B59	AF7	DDR1_DQ[59]	
M_DATA_B60	AH7	DDR1_DQ[60]	
M_DATA_B61	AH6	DDR1_DQ[61]	
M_DATA_B62	AE7	DDR1_DQ[62]	
M_DATA_B63	AF6	DDR1_DQ[63]	
	AR25	DDR1_ECC[0]	
	AR26	DDR1_ECC[1]	
	AM26	DDR1_ECC[2]	
	AM25	DDR1_ECC[3]	
	AP26	DDR1_ECC[4]	
	AP25	DDR1_ECC[5]	
	AL25	DDR1_ECC[6]	
	AL26	DDR1_ECC[7]	

DDR1_CKP[0]	AM20	CK_M_CH1_0_DP	12
DDR1_CKN[0]	AM21	CK_M_CH1_0_DN	12
DDR1_CKP[1]	AP22	CK_M_CH1_1_DP	12
DDR1_CKN[1]	AP21	CK_M_CH1_1_DN	12
DDR1_CKP[2]	AN20	CK_M_CH1_2_DP	12
DDR1_CKN[2]	AN21	CK_M_CH1_2_DN	12
DDR1_CKP[3]	AP19	CK_M_CH1_3_DP	12
DDR1_CKN[3]	AP20	CK_M_CH1_3_DN	12
DDR1_CKE[0]	AY29	M_SCKE_B0	12
DDR1_CKE[1]	AV29	M_SCKE_B1	12
DDR1_CKE[2]	AW29	M_SCKE_B2	12
DDR1_CKE[3]	AU29	M_SCKE_B3	12
DDR1_CS#[0]	AP17	M_SCS_B_N0	12
DDR1_CS#[1]	AN15	M_SCS_B_N1	12
DDR1_CS#[2]	AN17	M_SCS_B_N2	12
DDR1_CS#[3]	AM15	M_SCS_B_N3	12
DDR1_ODT[0]	AM16	M_ODT_B0	12
DDR1_ODT[1]	AL16	M_ODT_B1	12
DDR1_ODT[2]	AP15	M_ODT_B2	12
DDR1_ODT[3]	AL15	M_ODT_B3	12
DDR1_RAS#/DDR1_CAB[3]/DDR1_MA[16]	AN18	M_MAA_B16	
DDR1_WE#/DDR1_CAB[2]/DDR1_MA[14]	AL17	M_MAA_B14	
DDR1_CAS#/DDR1_CAB[1]/DDR1_MA[15]	AP16	M_MAA_B15	
DDR1_BA[0]/DDR1_CAB[4]/DDR1_BA[0]	AL18	M_SBS_B0	12
DDR1_BA[1]/DDR1_CAB[6]/DDR1_BA[1]	AM18	M_SBS_B1	12
DDR1_BA[2]/DDR1_CAA[5]/DDR1_BG[0]	AW28	M_BG_CH1_0	12
DDR1_MA[0]/DDR1_CAB[9]/DDR1_MA[0]	AL19	M_MAA_B0	
DDR1_MA[1]/DDR1_CAB[8]/DDR1_MA[1]	AL22	M_MAA_B1	
DDR1_MA[2]/DDR1_CAB[5]/DDR1_MA[2]	AM22	M_MAA_B2	
DDR1_MA[3]	AM23	M_MAA_B3	
DDR1_MA[4]	AP23	M_MAA_B4	
DDR1_MA[5]/DDR1_CAA[0]/DDR1_MA[5]	AL23	M_MAA_B5	
DDR1_MA[6]/DDR1_CAA[2]/DDR1_MA[6]	AW26	M_MAA_B6	
DDR1_MA[7]/DDR1_CAA[4]/DDR1_MA[7]	AY26	M_MAA_B7	
DDR1_MA[8]/DDR1_CAA[3]/DDR1_MA[8]	AU26	M_MAA_B8	
DDR1_MA[9]/DDR1_CAA[1]/DDR1_MA[9]	AW27	M_MAA_B9	
DDR1_MA[10]/DDR1_CAB[7]/DDR1_MA[10]	AP18	M_MAA_B10	
DDR1_MA[11]/DDR1_CAA[7]/DDR1_MA[11]	AU27	M_MAA_B11	
DDR1_MA[12]/DDR1_CAA[6]/DDR1_MA[12]	AV27	M_MAA_B12	
DDR1_MA[13]/DDR1_CAB[0]/DDR1_MA[13]	AR15	M_MAA_B13	
DDR1_MA[14]/DDR1_CAA[9]/DDR1_BG[1]	AY28	M_BG_CH1_1	12
DDR1_MA[15]/DDR1_CAA[8]/DDR1_ACT#	AU28	DDR_CH1_ACT_N	12
DDR1_PAR	AL20	DDR_CH1_PAR	12
DDR1_ALERT#	AY25	DDR_CH1_ALERT_N	12
DDR1_DQSN[0]/DDR0_DQSN[2]	AF34	M_DQS_B_DN0	12
DDR1_DQSN[1]/DDR0_DQSN[3]	AK33	M_DQS_B_DN1	12
DDR1_DQSN[2]/DDR0_DQSN[6]	AN33	M_DQS_B_DN2	12
DDR1_DQSN[3]/DDR0_DQSN[7]	AN29	M_DQS_B_DN3	12
DDR1_DQSN[4]/DDR1_DQSN[2]	AN13	M_DQS_B_DN4	12
DDR1_DQSN[5]/DDR1_DQSN[3]	AR8	M_DQS_B_DN5	12
DDR1_DQSN[6]	AM8	M_DQS_B_DN6	12
DDR1_DQSN[7]	AG6	M_DQS_B_DN7	12
DDR1_DQSP[0]/DDR0_DQSP[2]	AF35	M_DQS_B_DP0	12
DDR1_DQSP[1]/DDR0_DQSP[3]	AL33	M_DQS_B_DP1	12
DDR1_DQSP[2]/DDR0_DQSP[6]	AP33	M_DQS_B_DP2	12
DDR1_DQSP[3]/DDR0_DQSP[7]	AN28	M_DQS_B_DP3	12
DDR1_DQSP[4]/DDR1_DQSP[2]	AN12	M_DQS_B_DP4	12
DDR1_DQSP[5]/DDR1_DQSP[3]	AP8	M_DQS_B_DP5	12
DDR1_DQSP[6]	AL8	M_DQS_B_DP6	12
DDR1_DQSP[7]	AG7	M_DQS_B_DP7	12
DDR1_DQSP[8]	AN25		
DDR1_DQSN[8]	AN26		
DDR_VREF_CA	AB40	DDR_VREF_CA	11
DDR0_VREF_DQ	AC40	DDR0_VREF_DQ	11
DDR1_VREF_DQ	AC39	DDR1_VREF_DQ	12

M_MAA_B[0..16] 12

2 OF 12

LGA 1151 SOCKET

DDR3 & 4 COLAY

DDR_CH1_ALERT_N

Q8
NX7002AK SOT23

+5V_DUAL

R16
4.7K 0402

DDR4_PLUG 6,11,12,38

DDR_VREF_CA

CC1
0.01UF 25V X7R 0402

DDR0_VREF_DQ

CC37
0.01UF 25V X7R 0402

DDR1_VREF_DQ

CC39
0.01UF 25V X7R 0402

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Title	CPU DDR4 CHANNEL B		
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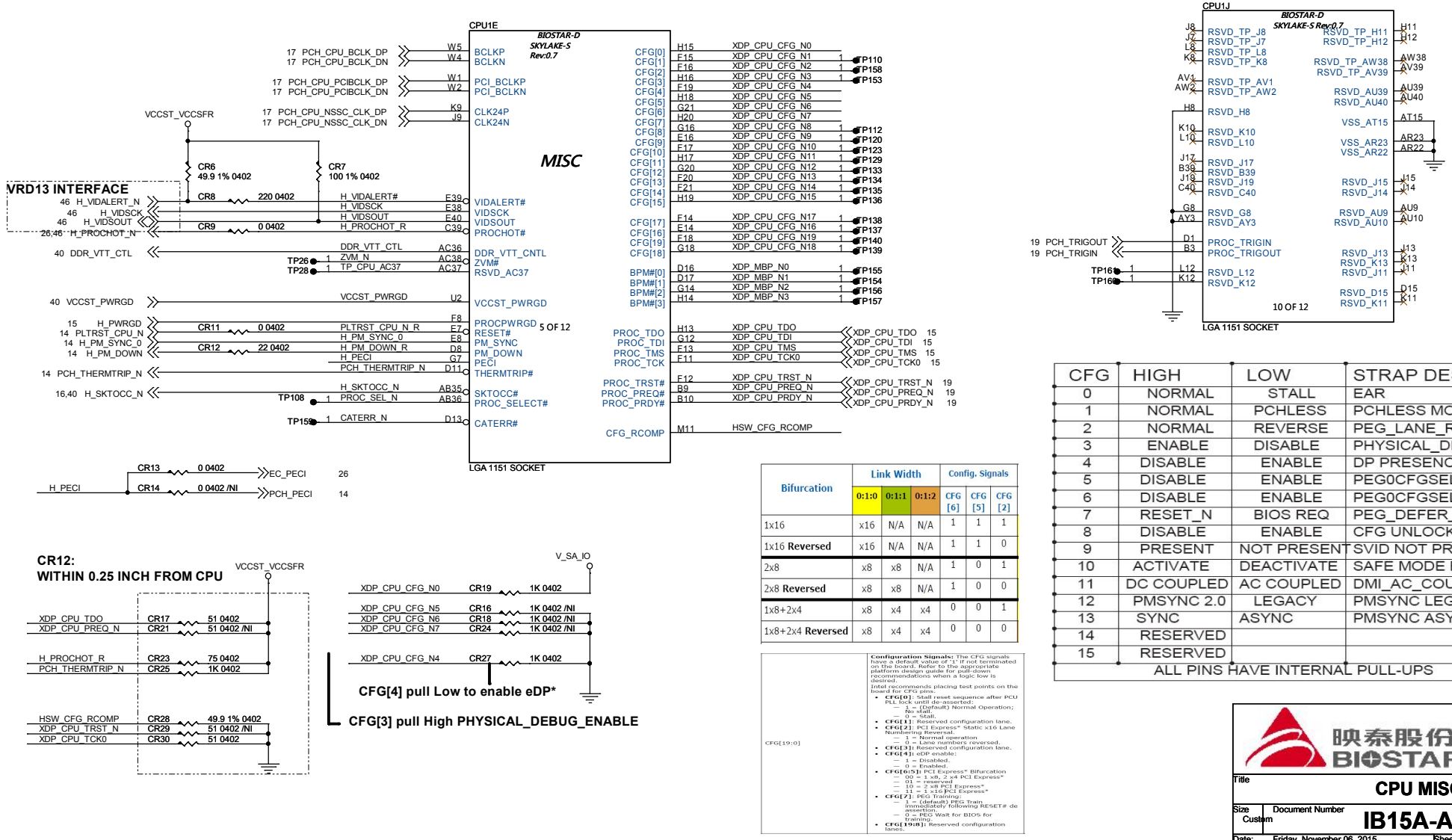

Bifurcation	Link Width			Config. Signals		
	0:1:0	0:1:1	0:1:2	CFG [6]	CFG [5]	CFG [2]
1x16	x16	N/A	N/A	1	1	1
1x16 **Reversed**	x16	N/A	N/A	1	1	0
2x8	x8	x8	N/A	1	0	1
2x8 **Reversed**	x8	x8	N/A	1	0	0
1x8+2x4	x8	x4	x4	0	0	1
1x8+2x4 **Reversed**	x8	x4	x4	0	0	0

CFG[19:0]

Configuration Signals: The CFG signals have a default value of '1' if not terminated on the board. Refer to the appropriate platform design guide for pull-down recommendations when a logic low is desired.
Intel recommends placing test points on the board for CFG pins.

- **CFG[0]:** Stall reset sequence after PCU PLL lock until de-asserted;
  - 1 = (Default) Normal Operation; No stall.
  - 0 = Stall.
- **CFG[1]:** Reserved configuration lane.
- **CFG[2]:** PCI Express* Static x16 Lane Numbering Reversal.
  - 1 = Normal operation
  - 0 = Lane numbers reversed.
- **CFG[3]:** Reserved configuration lane.
- **CFG[4]:** eDP enable:
  - 1 = Disabled.
  - 0 = Enabled.
- **CFG[6:5]:** PCI Express* Bifurcation
  - 00 = 1 x8, 2 x4 PCI Express*
  - 01 = reserved
  - 10 = 2 x8 PCI Express*
  - 11 = 1 x16 PCI Express*
- **CFG[7]:** PEG Training:
  - 1 = (default) PEG Train immediately following RESET# de assertion.
  - 0 = PEG Wait for BIOS for training.
- **CFG[19:8]:** Reserved configuration lanes.

CFG	HIGH	LOW	STRAP DESCRIPTION
0	NORMAL	STALL	EAR
1	NORMAL	PCHLESS	PCHLESS MODE
2	NORMAL	REVERSE	PEG_LANE_REVERSAL
3	ENABLE	DISABLE	PHYSICAL_DEBUG_ENABLE
4	DISABLE	ENABLE	DP PRESENCE
5	DISABLE	ENABLE	PEG0CFGSEL[0]
6	DISABLE	ENABLE	PEG0CFGSEL[1]
7	RESET_N	BIOS REQ	PEG_DEFER_TRAINING
8	DISABLE	ENABLE	CFG UNLOCK
9	PRESENT	NOT PRESENT	SVID NOT PRESENT
10	ACTIVATE	DEACTIVATE	SAFE MODE BOOT
11	DC COUPLED	AC COUPLED	DMI_AC_COUPLED
12	PMSYNC 2.0	LEGACY	PMSYNC LEGACY
13	SYNC	ASYNC	PMSYNC ASYNC MODE
14	RESERVED		
15	RESERVED		

ALL PINS HAVE INTERNAL PULL-UPS

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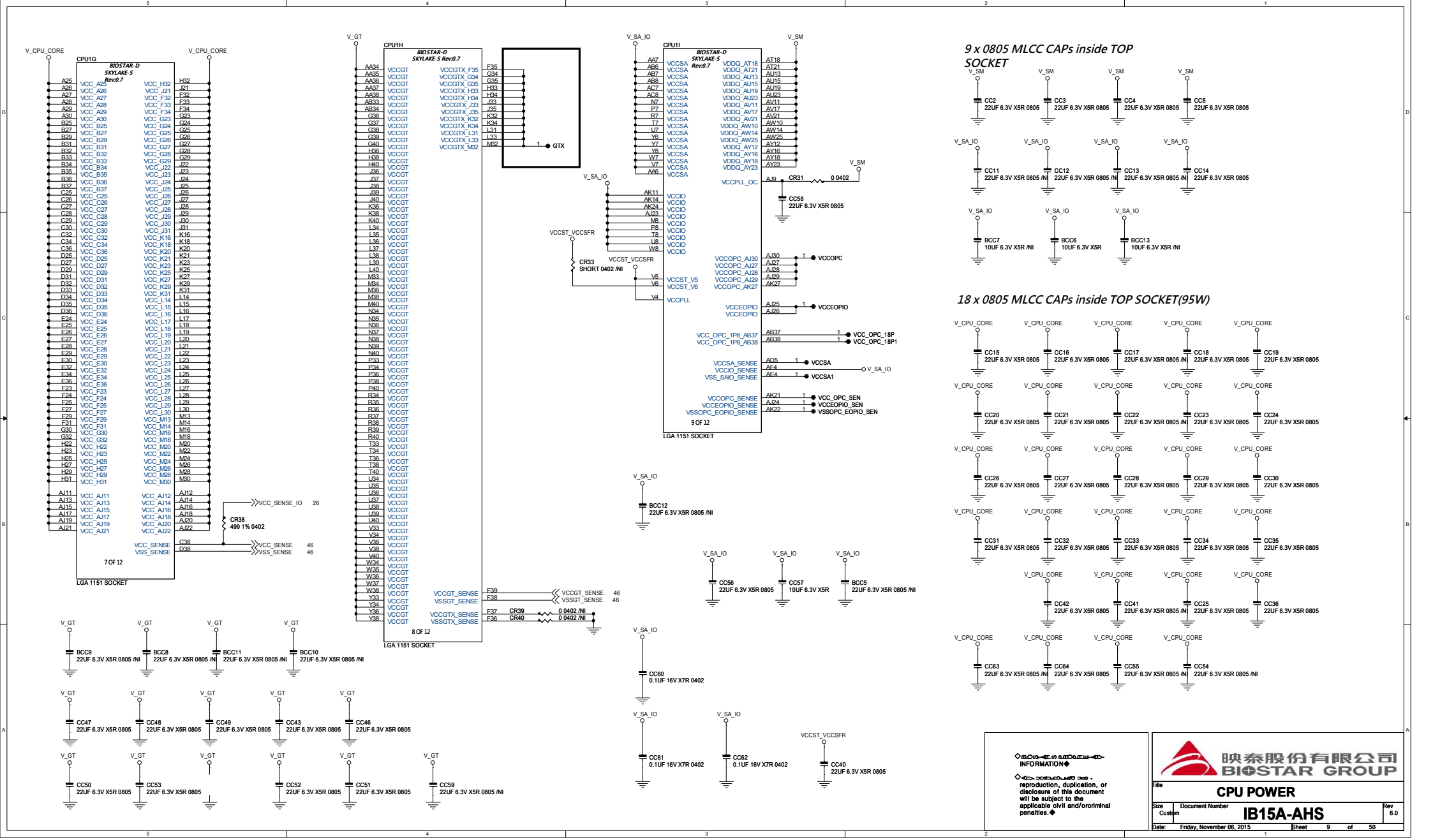

9 x 0805 MLCC CAPs inside TOP SOCKET

18 x 0805 MLCC CAPs inside TOP SOCKET(95W)

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Title	CPU POWER	
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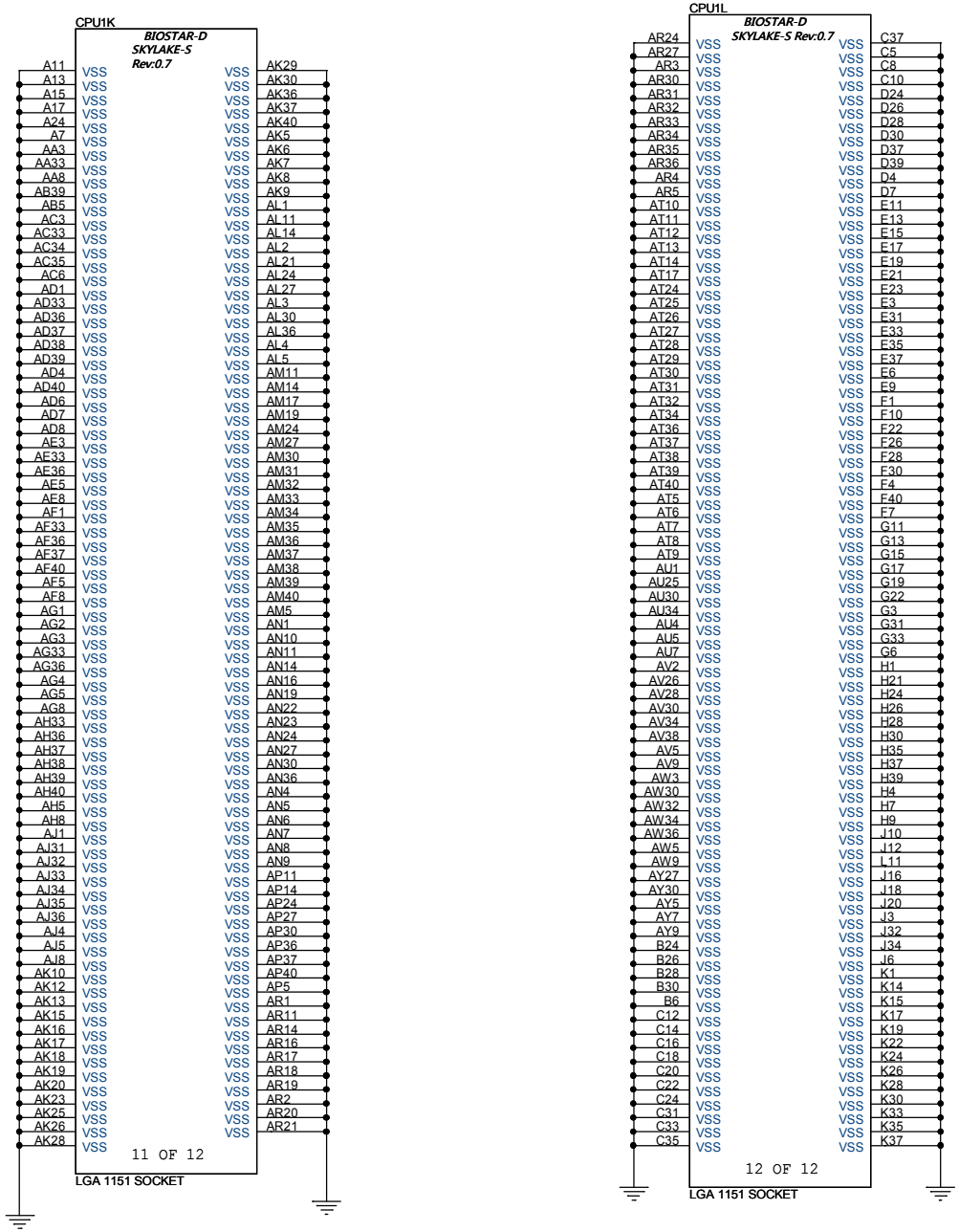

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Title: CPU GND

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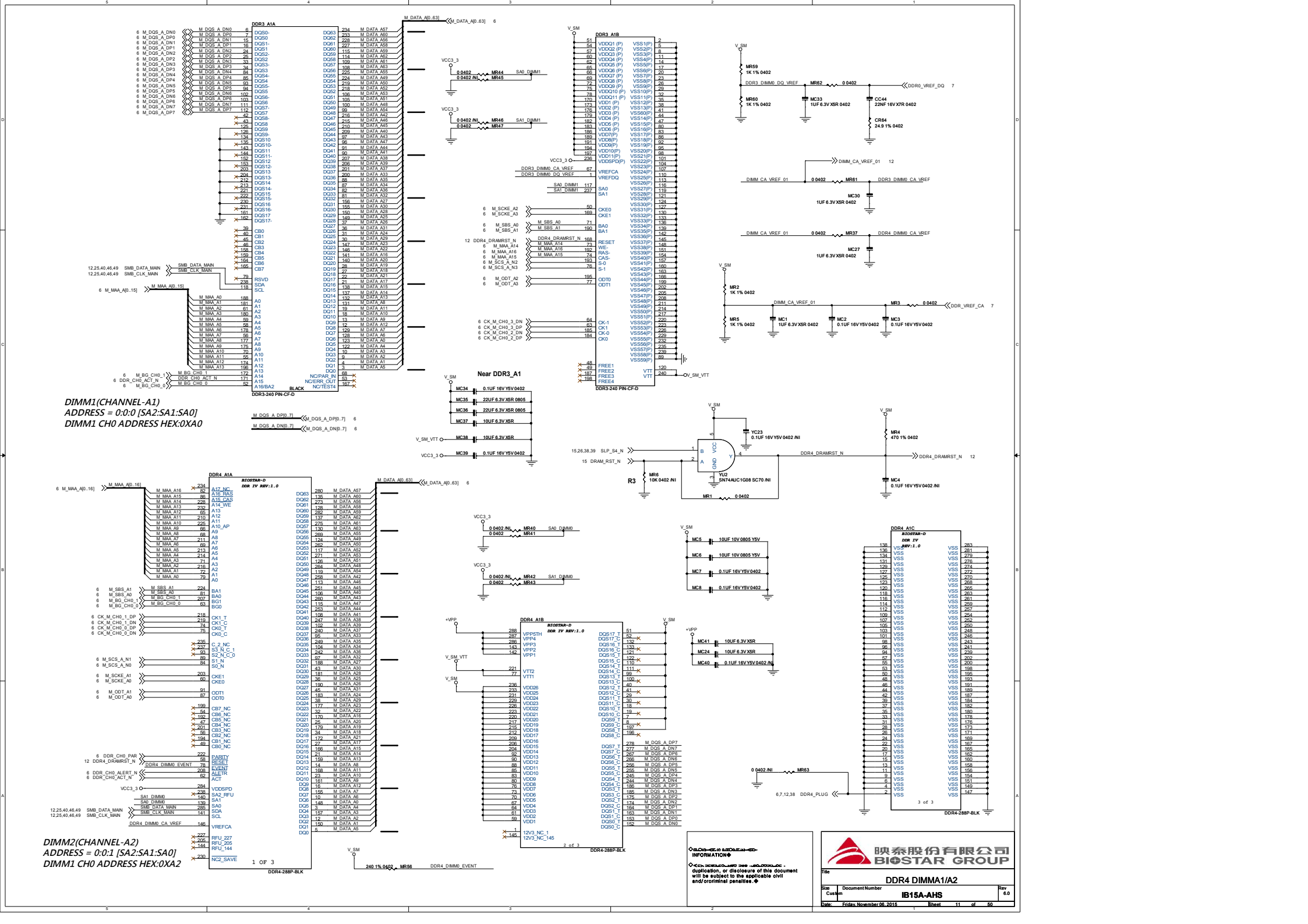
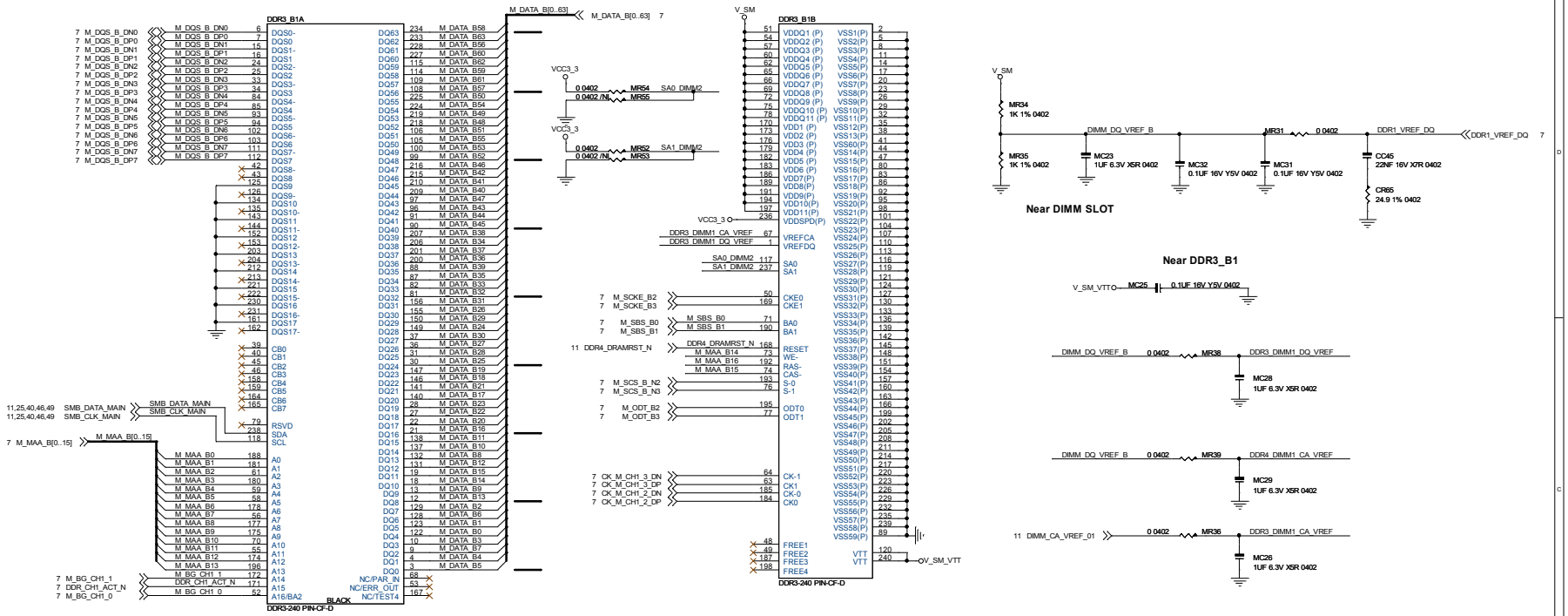
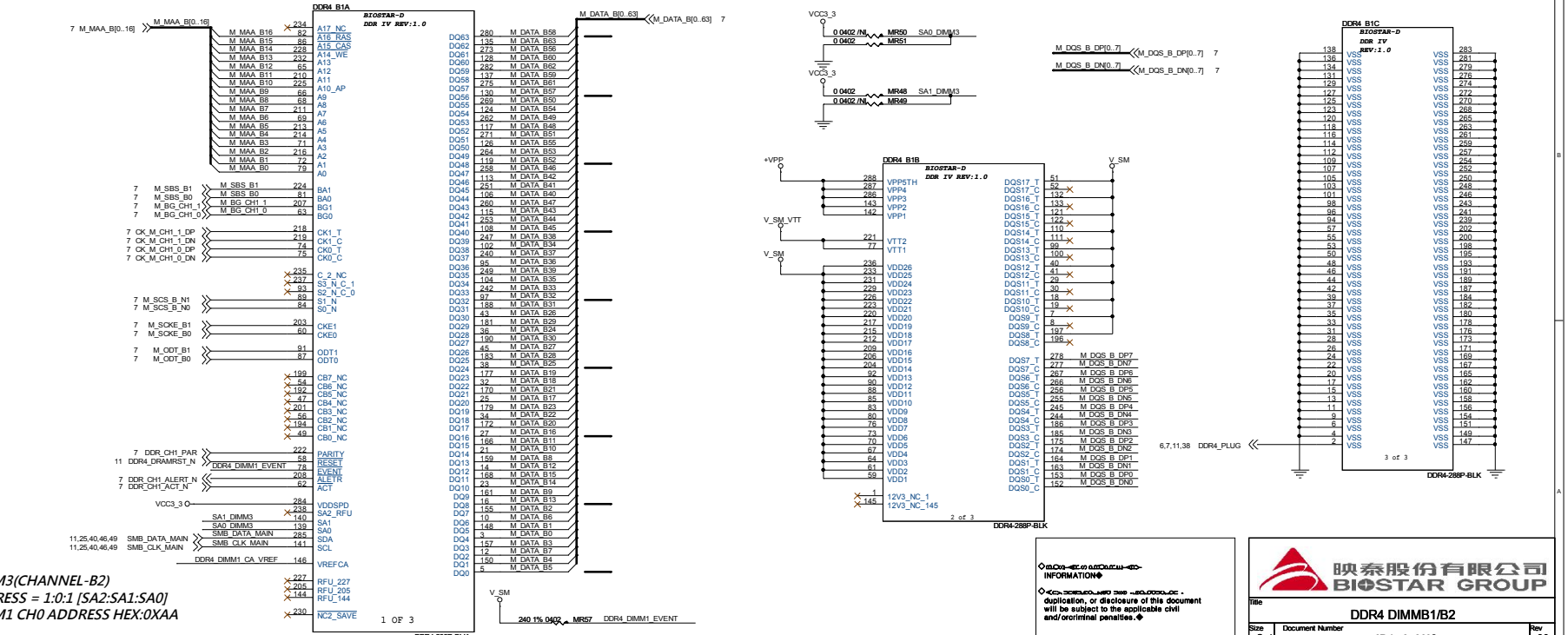

DDR3_A1A
DDR3-240 PIN-CF-D
DDR3_A1B
DDR3-240 PIN-CF-D
Near DDR3_A1
DIMM1(CHANNEL-A1)
ADDRESS = 0:0:0 [SA2:SA1:SA0]
DIMM1 CH0 ADDRESS HEX:0XA0
DDR4_A1A
DDR4-288P-BLK
DDR4_A1B
DDR4-288P-BLK
DDR4_A1C
DDR4-288P-BLK
DIMM2(CHANNEL-A2)
ADDRESS = 0:0:1 [SA2:SA1:SA0]
DIMM1 CH0 ADDRESS HEX:0XA2
INFORMATION
DDR4 DIMMA1/A2
IB15A-AHS
Friday, November 06, 2015



DIMM3(CHANNEL-B1)
ADDRESS = 0:0:1 [SA2:SA1:SA0]
DIMM1 CH0 ADDRESS HEX:0XA8



DIMM3(CHANNEL-B2)
ADDRESS = 1:0:1 [SA2:SA1:SA0]
DIMM1 CH0 ADDRESS HEX:0XAA

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Title: DDR4 DIMMB1/B2

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Custom	IB15A-AHS	6.0

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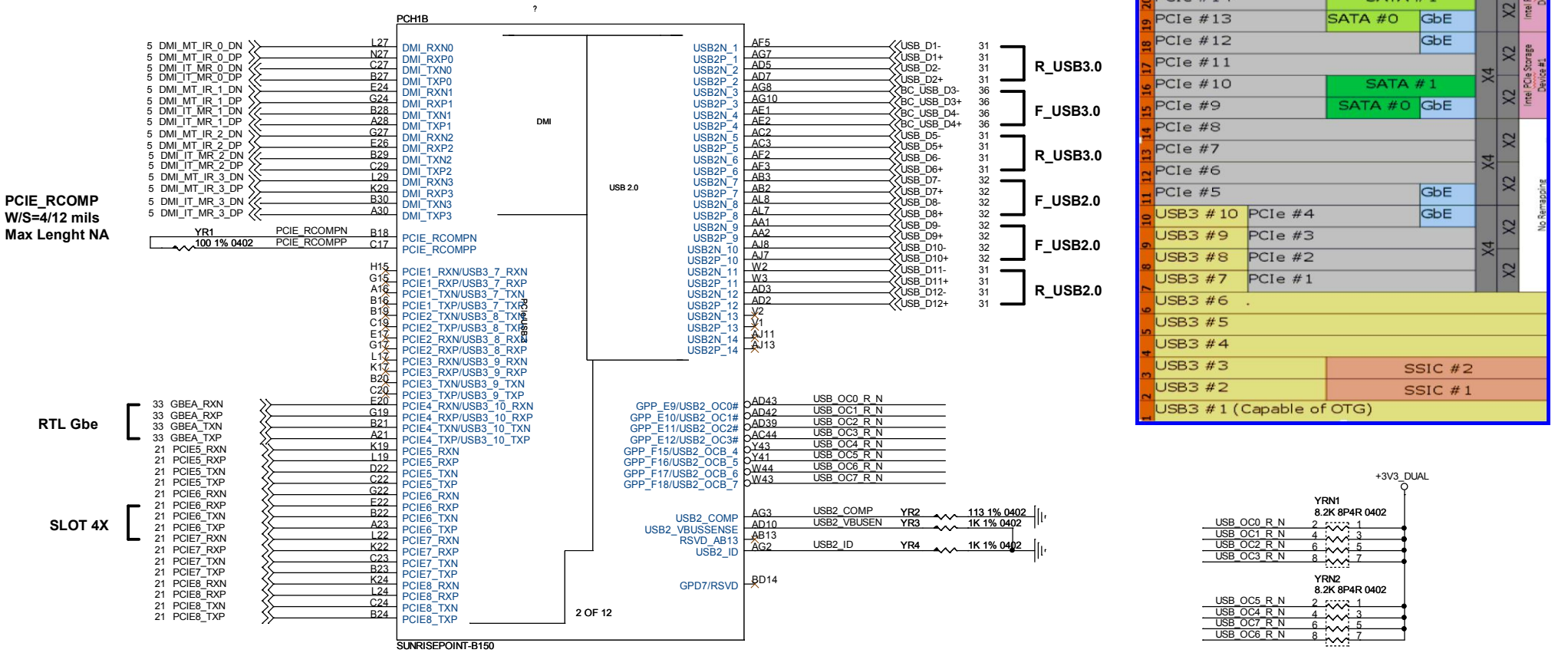
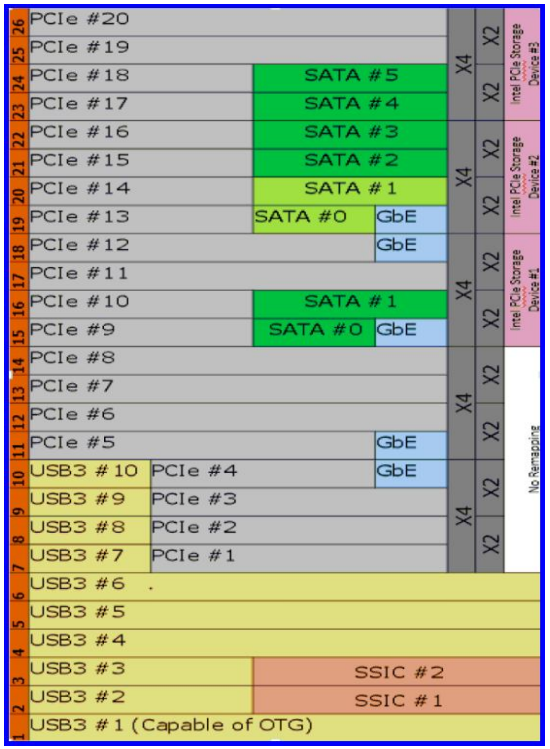
PCH PART: Y+Reference





Title	PCH DMI/PCIE/USB		
Size B	Document Number IB15A-AHS		Rev 6.0
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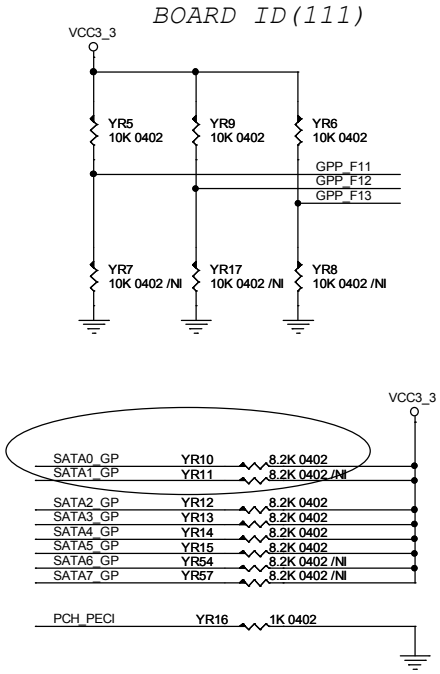
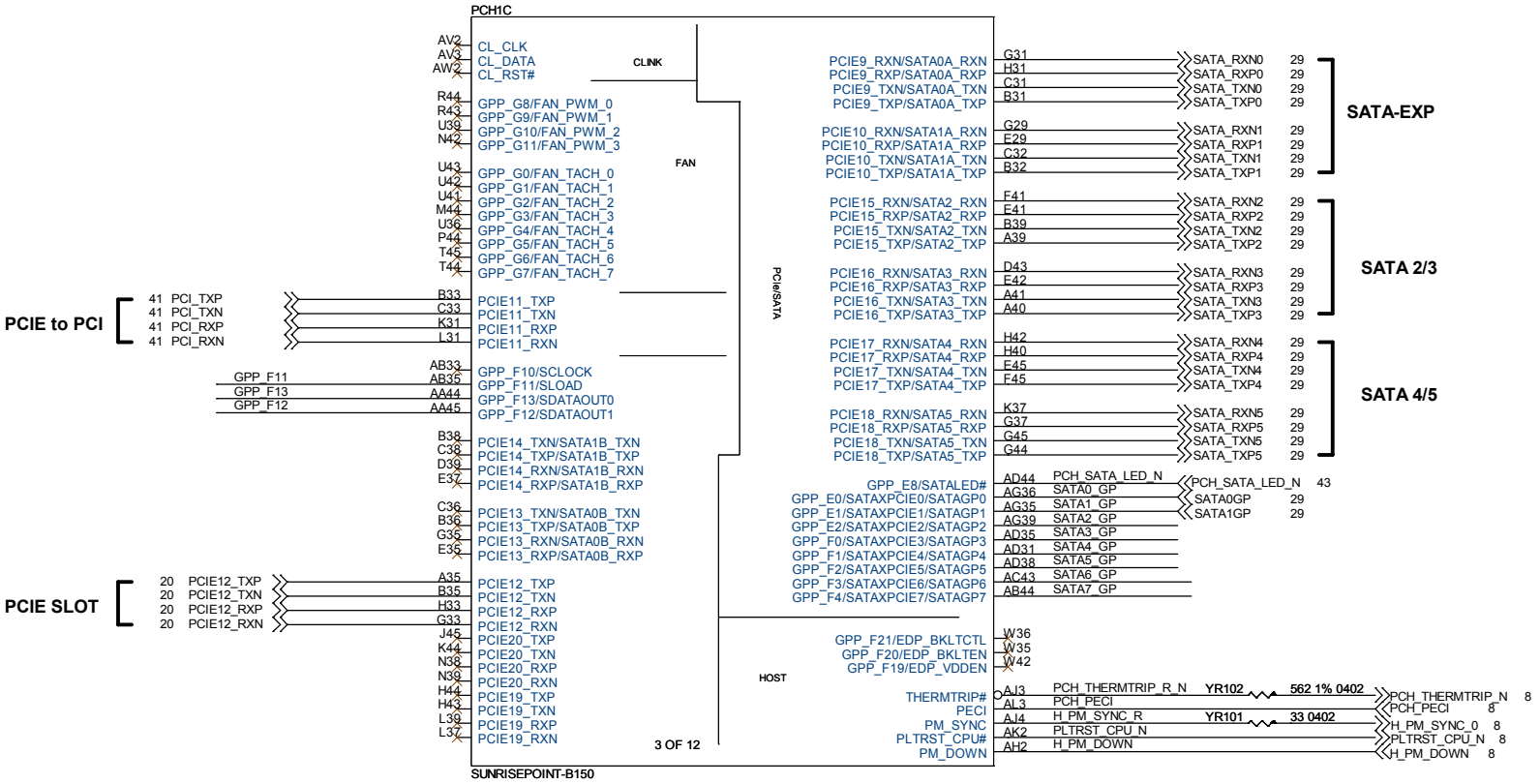
PCH PART: Y+Reference





GbE can be mapped into one of the PCIe Ports 4-5, Port 9, and Ports 12-13.

29 SATA_RXP2
29 SATA_RXN2
29 SATA_TXN2
29 SATA_TXP2

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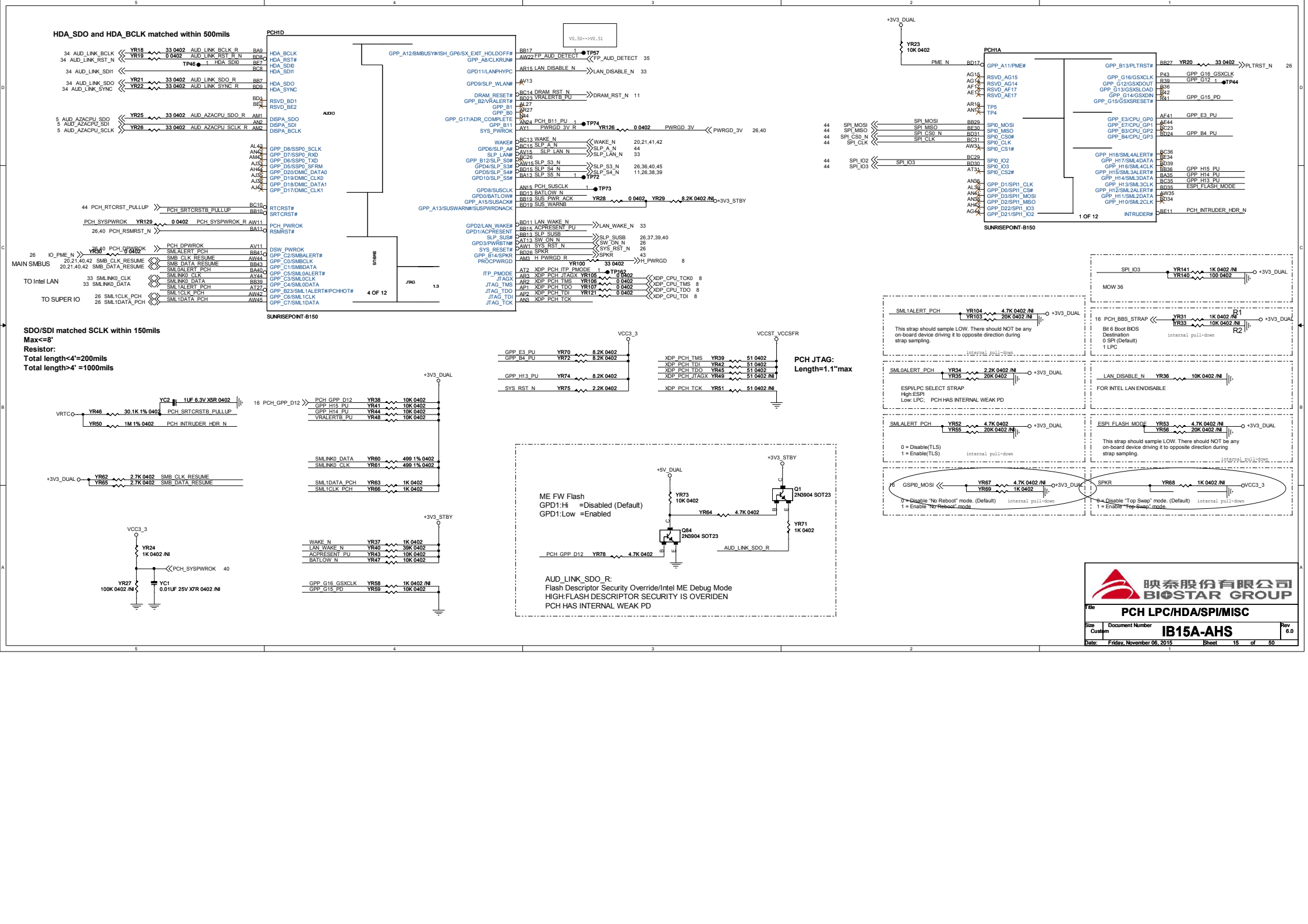
Title	PCH CLINK/SATA/CPU HOST	
Size B	Document Number IB15A-AHS	Rev 6.0
Date: Friday, November 06, 2015	Sheet 14 of 50	



Title	PCH LPC/HDA/SPI/MISC
Size	Custom
Document Number	IB15A-AHS
Rev	6.0
Date:	Friday, November 06, 2015
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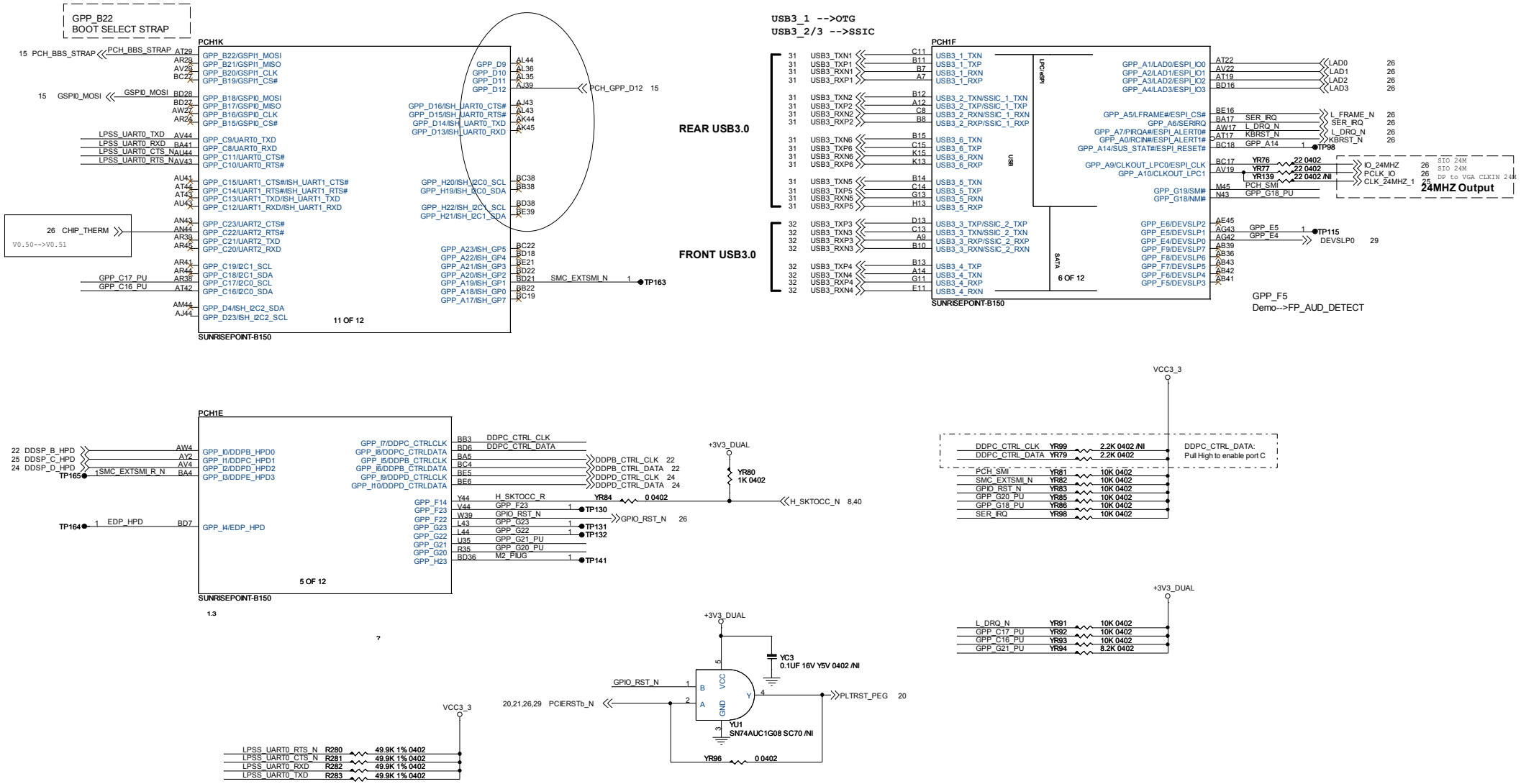
PCH PART: Y+Reference



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Title: PCH LPC/DP/USB3/UART

Size: Custom | Document Number: IB15A-AHS | Rev: 6.0

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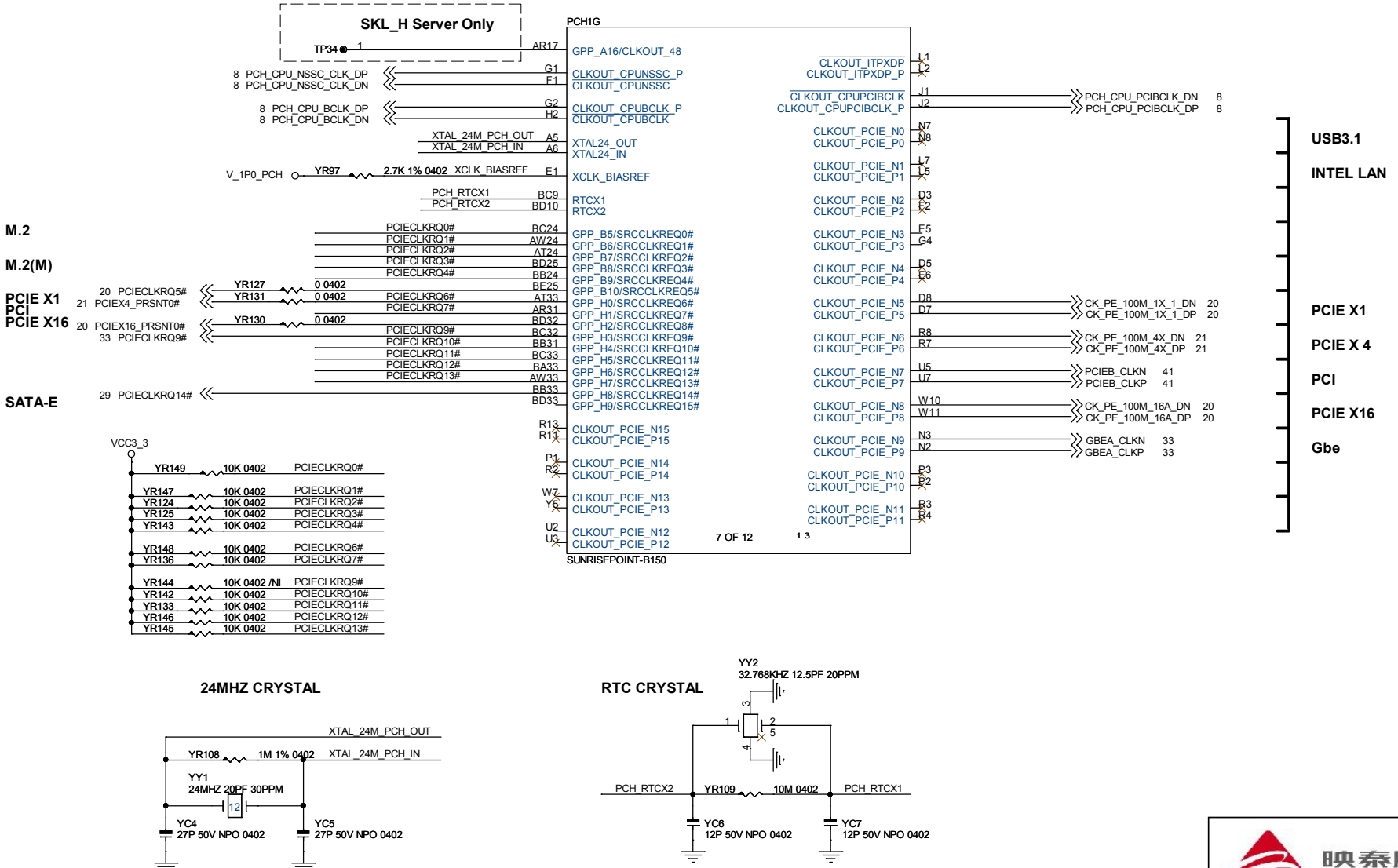

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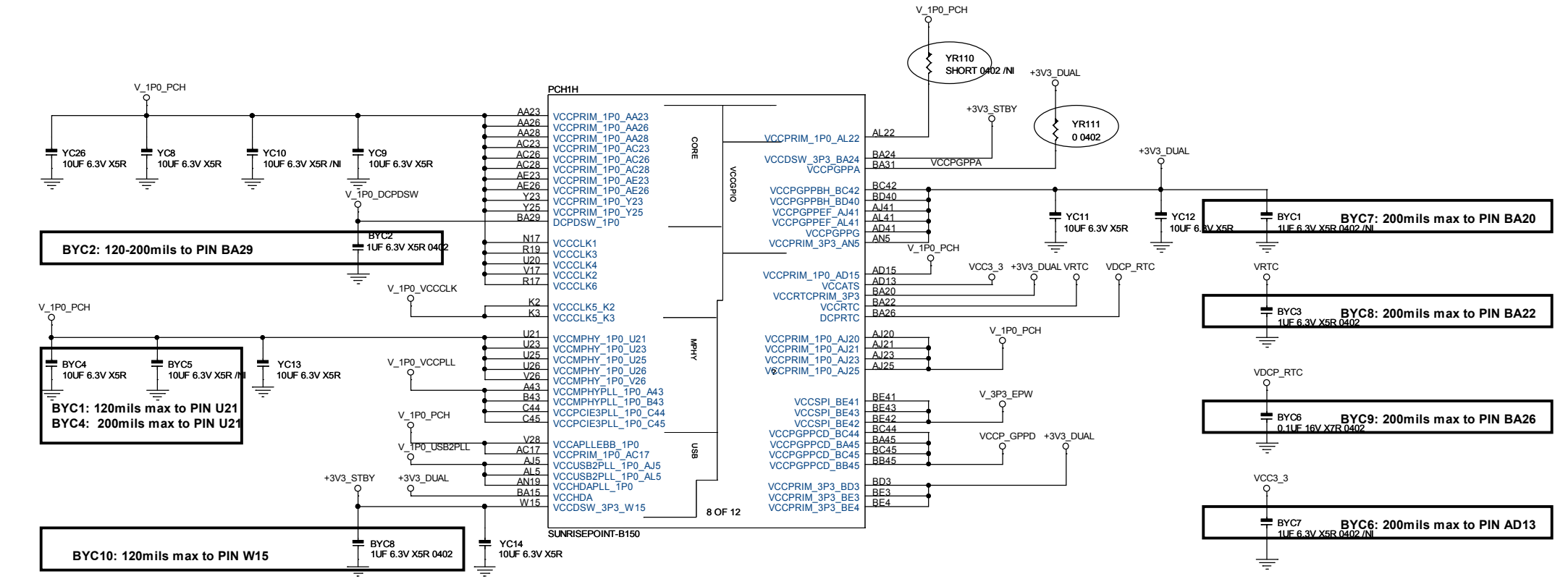
Title	PCH CLOCK BUFFER	
Size B	Document Number IB15A-AHS	Rev 6.0
Date: Friday, November 06, 2015	Sheet 17 of 50	



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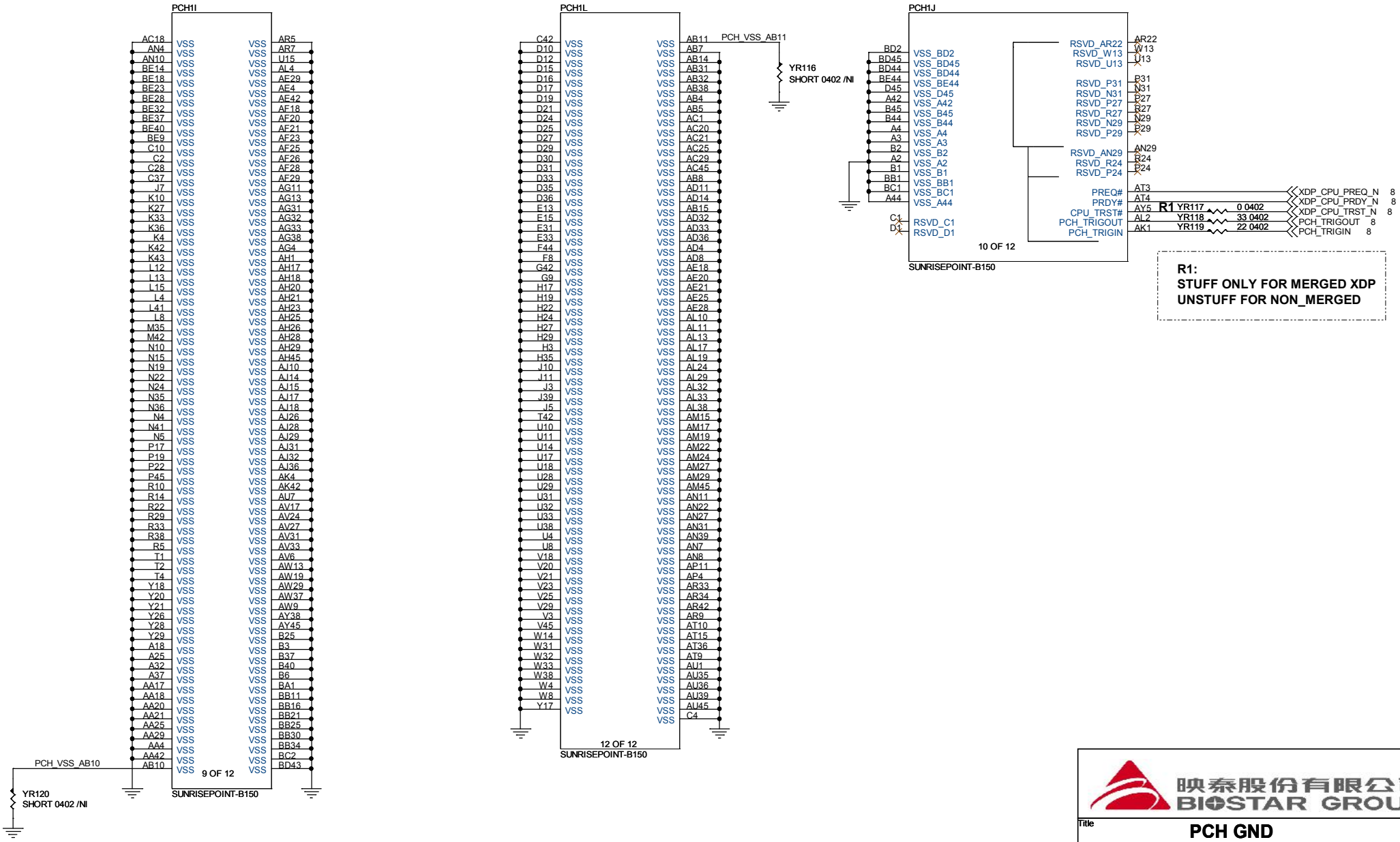
Title	PCH POWER	
Size B	Document Number IB15A-AHS	Rev 6.0
Date: Friday, November 06, 2015	Sheet 18 of 50	



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Title	PCH GND	
Size B	Document Number IB15A-AHS	Rev 6.0
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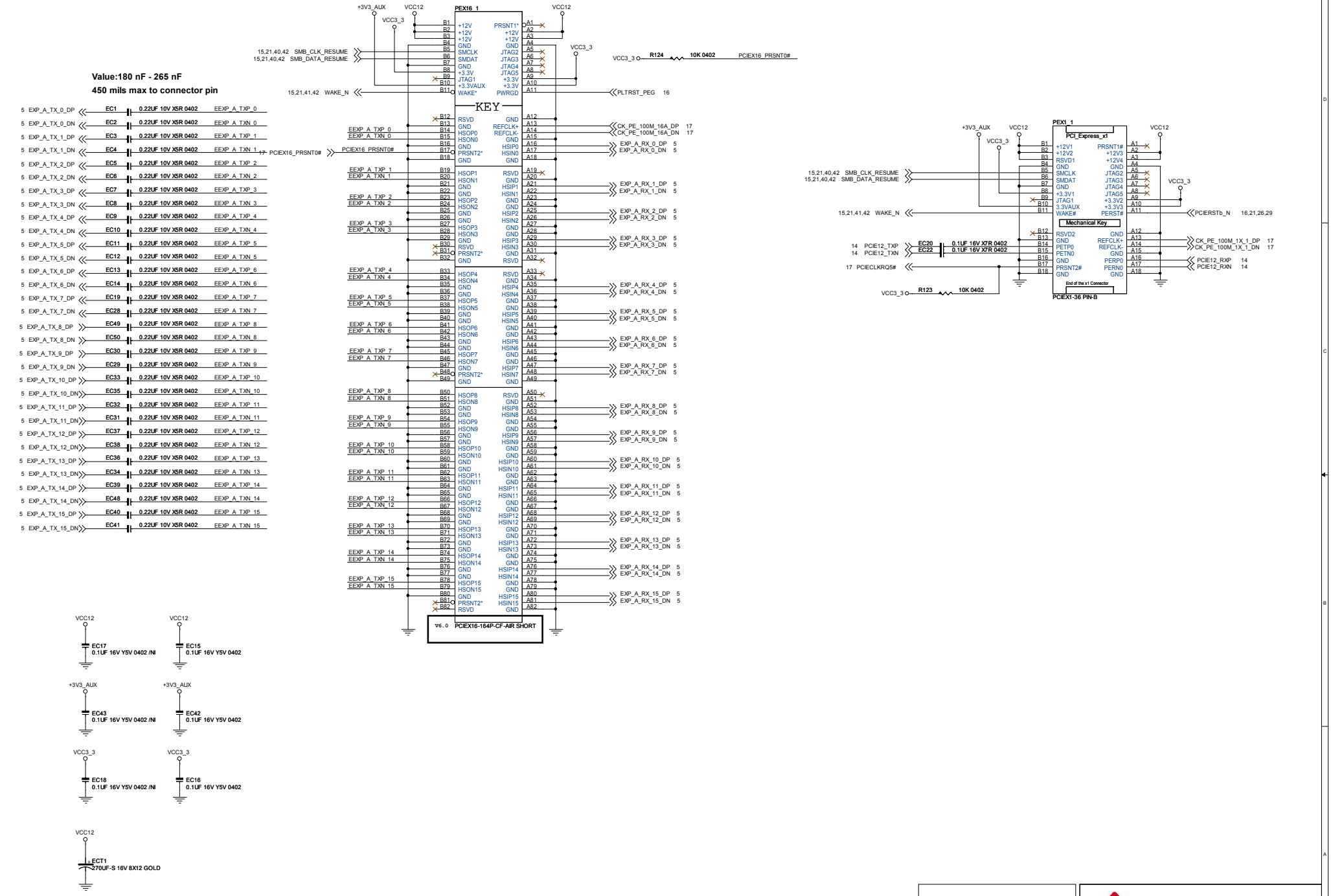
SLOT PART: E+Reference



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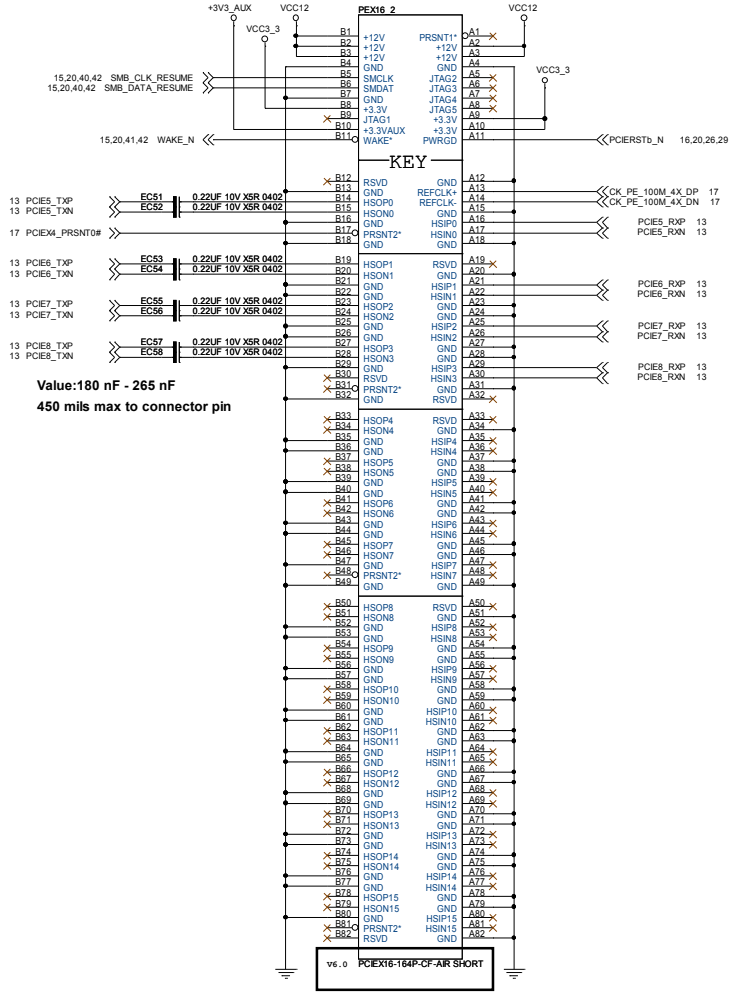
Title	PCIEX16 SLOT 1 & 2		
Size C	Document Number IB15A-AHS		Rev 6.0
Date: Friday, November 06, 2015	Sheet 20 of 50		

SLOT PART: E+Reference



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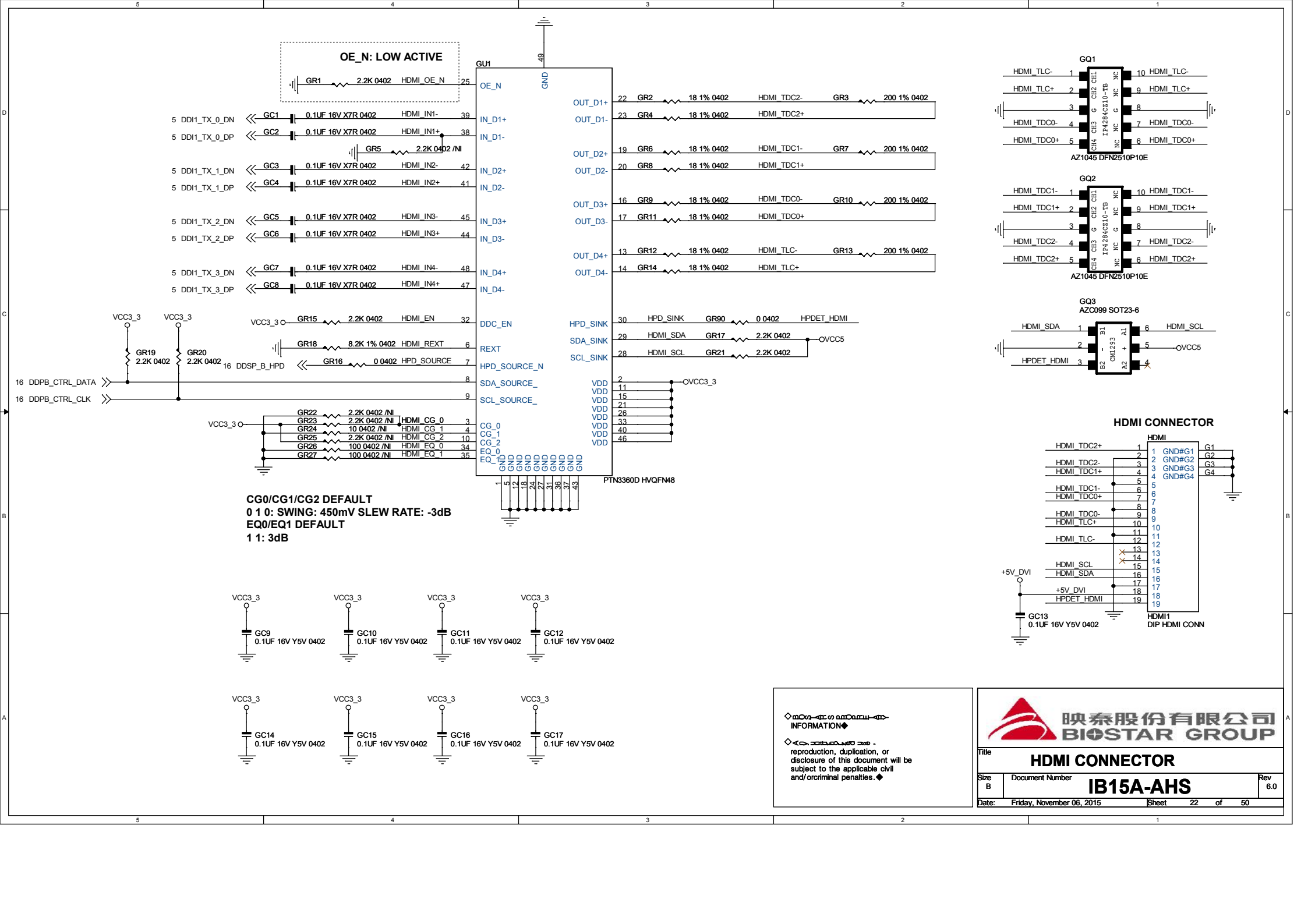
Title	PCIEX4 SLOT & mPCIE	
Size C	Document Number IB15A-AHS	Rev 6.0
Date: Friday, November 06, 2015	Sheet 21 of 50	



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Title	HDMI CONNECTOR	
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Title: DP CONNECTOR

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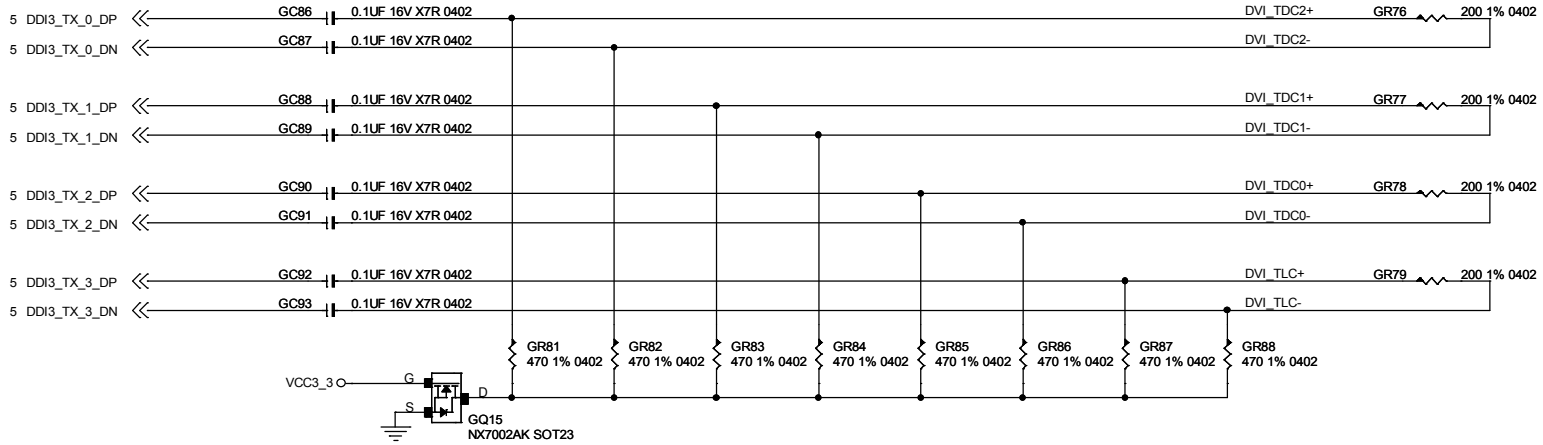
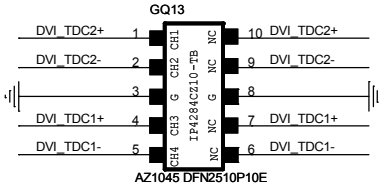
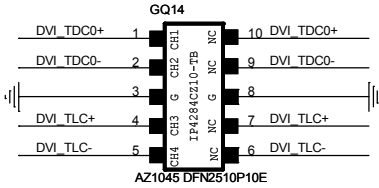
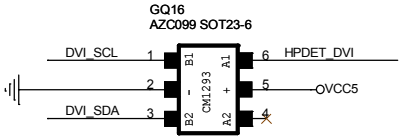
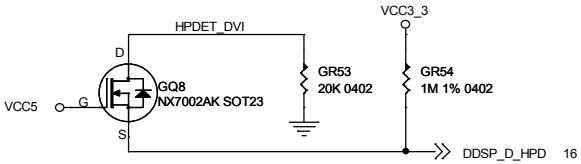


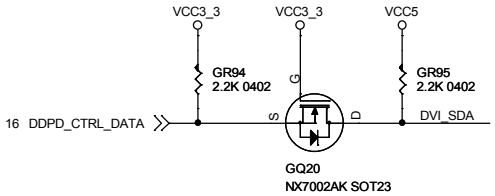


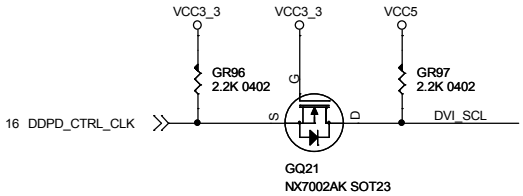


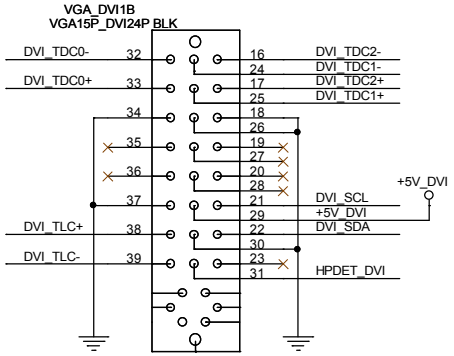




LEVEL SHIFTER
HPD +5V SWITCH TO +3.3V







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Title	DVI	
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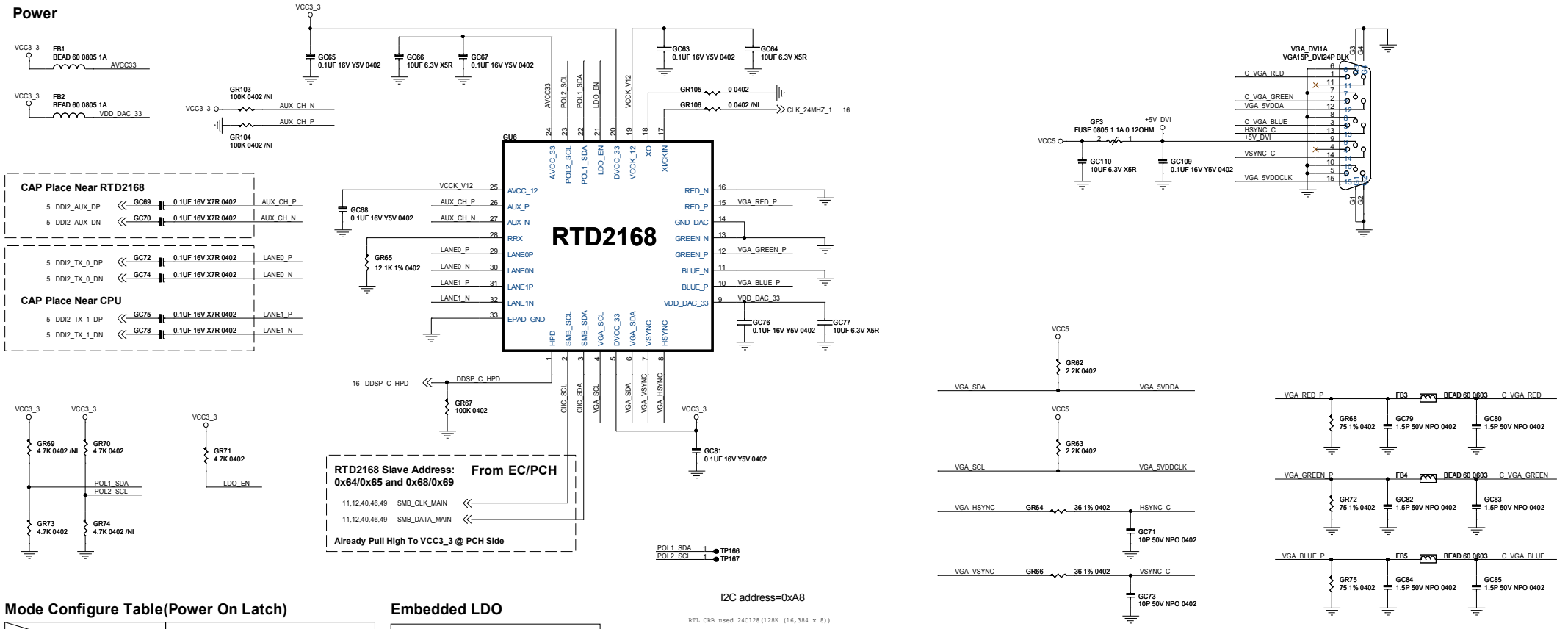

Mode Configure Table(Power On Latch)

		POL1_SDA(PIN22)	
		0	1
POL2_SCL(PIN23)	0	X	EP MODE
	1	ROM ONLY MODE	**EEPROM MODE**

Embedded LDO

LDO_EN(PIN21)	
0	1
VCCK_V12 from External 1.2V	**VCCK_V12 from Embedded LDO**

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Title: **RTD2168 EDP to VGA**

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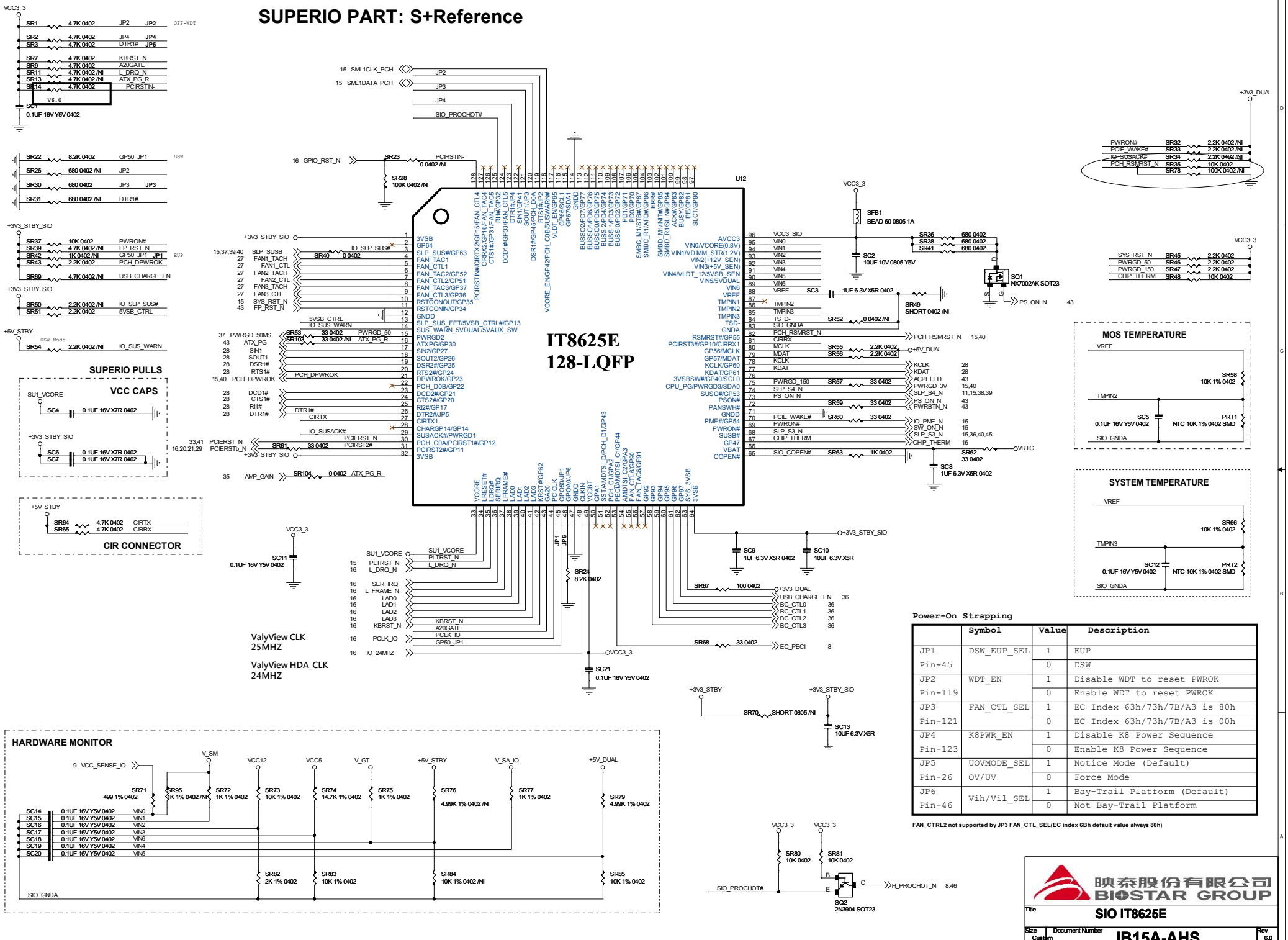
SUPERIO PART: S+Reference



Power-On Strapping

	Symbol	Value	Description
JP1	DSW_EUP_SEL	1	EUP
Pin-45		0	DSW
JP2	WDT_EN	1	Disable WDT to reset PWROK
Pin-119		0	Enable WDT to reset PWROK
JP3	FAN_CTL_SEL	1	EC Index 63h/73h/7B/A3 is 80h
Pin-121		0	EC Index 63h/73h/7B/A3 is 00h
JP4	K8PWR_EN	1	Disable K8 Power Sequence
Pin-123		0	Enable K8 Power Sequence
JP5	UOVMODE_SEL	1	Notice Mode (Default)
Pin-26	OV/UV	0	Force Mode
JP6	Vih/Vil_SEL	1	Bay-Trail Platform (Default)
Pin-46		0	Not Bay-Trail Platform

FAN_CTRL2 not supported by JP3 FAN_CTL_SEL(EC index 6Bh default value always 80h)

Title	SIO IT8625E
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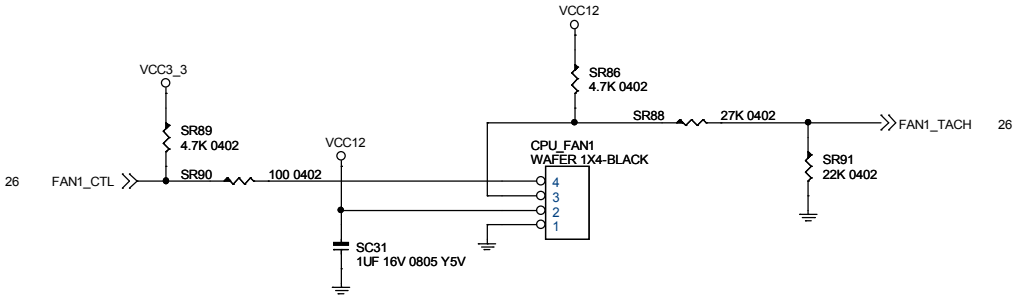

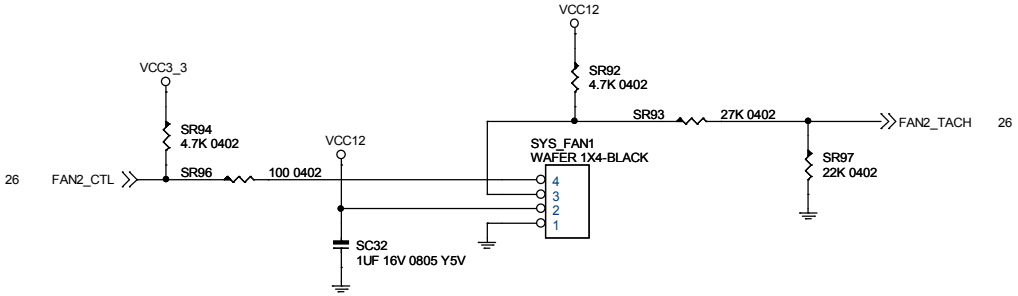

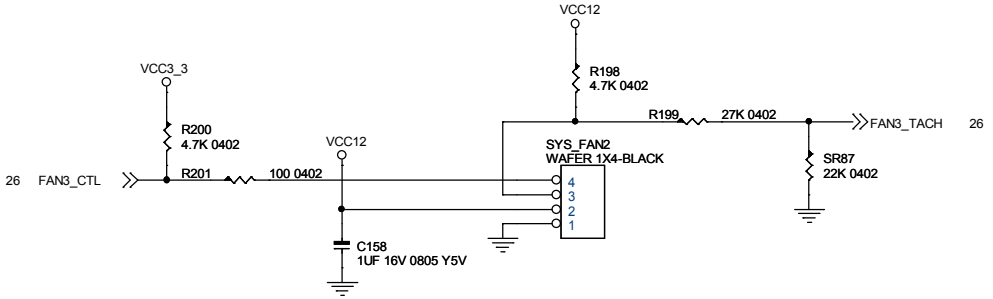

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Title	FAN & PS2	
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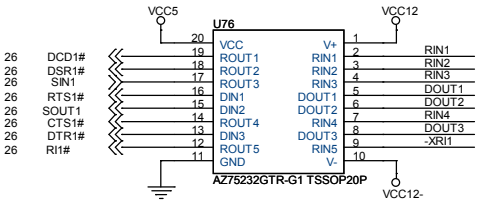
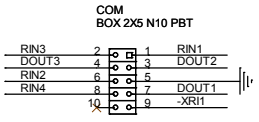
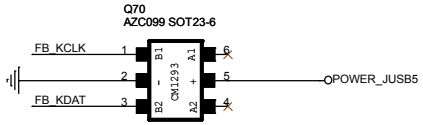
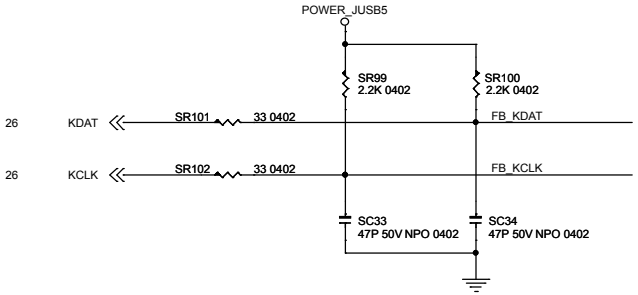


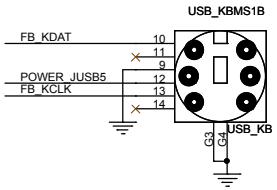


COM PORT

WAKE ON RING







KEYBOARD & MOUSE

PARALLEL CONNECTOR

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Title: COM1 / PS2 CONN

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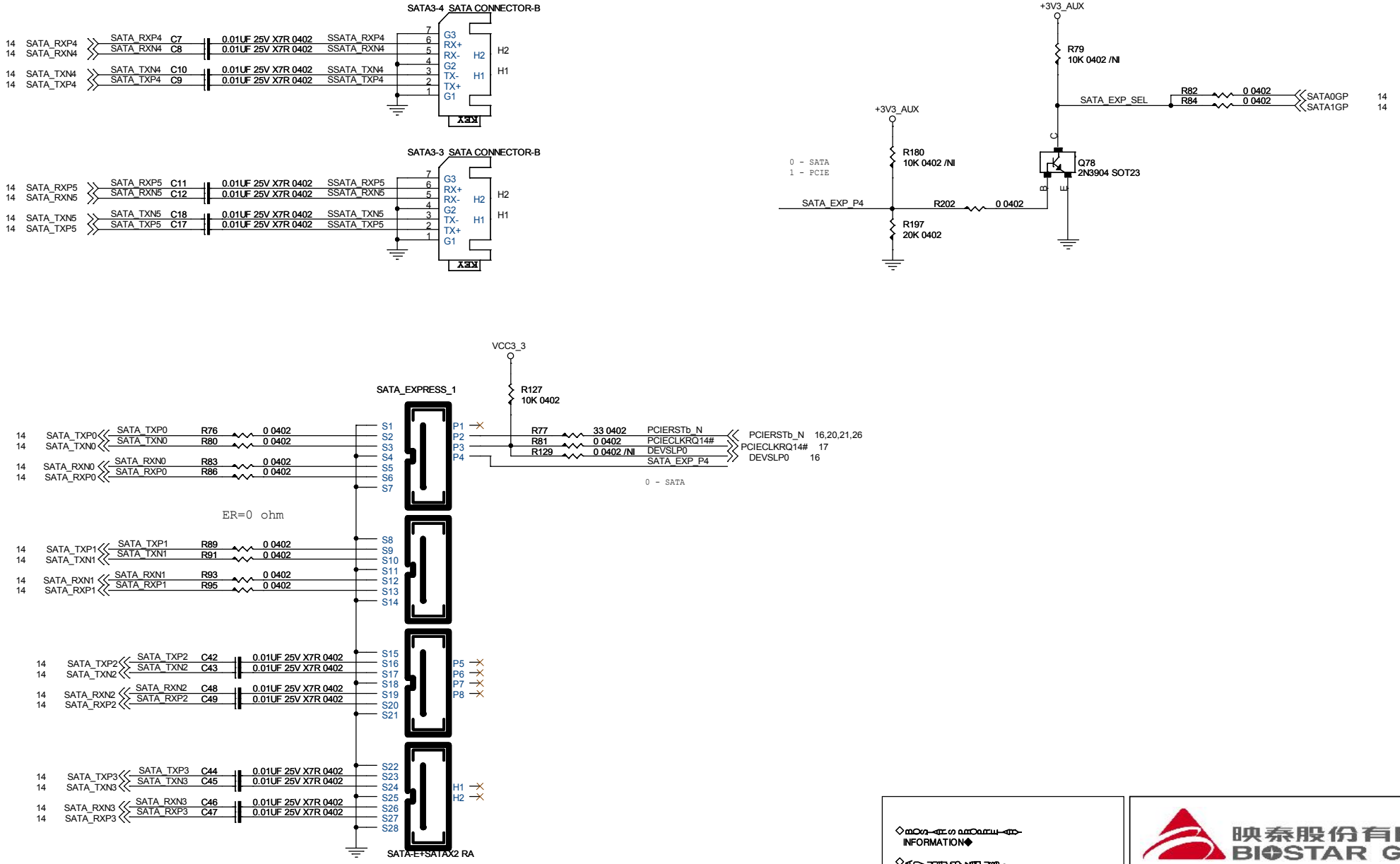

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Title: **M.2 CONNECTOR**

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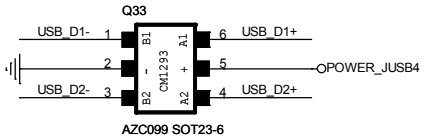

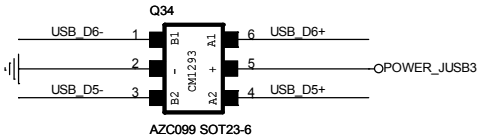

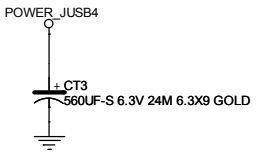

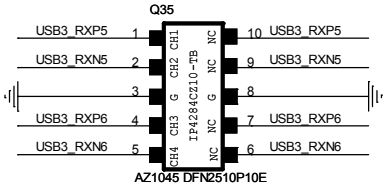

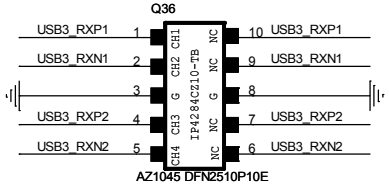

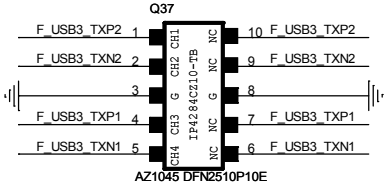

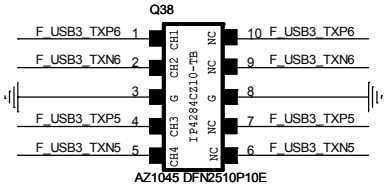

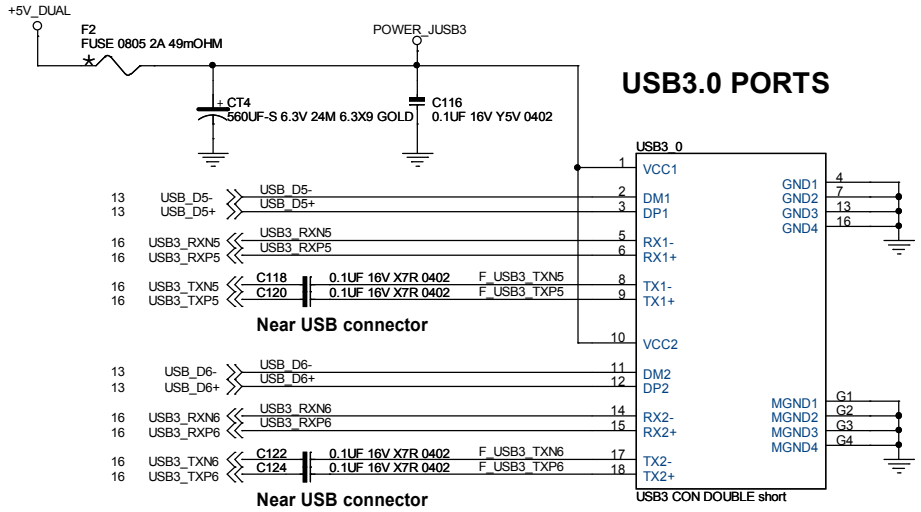

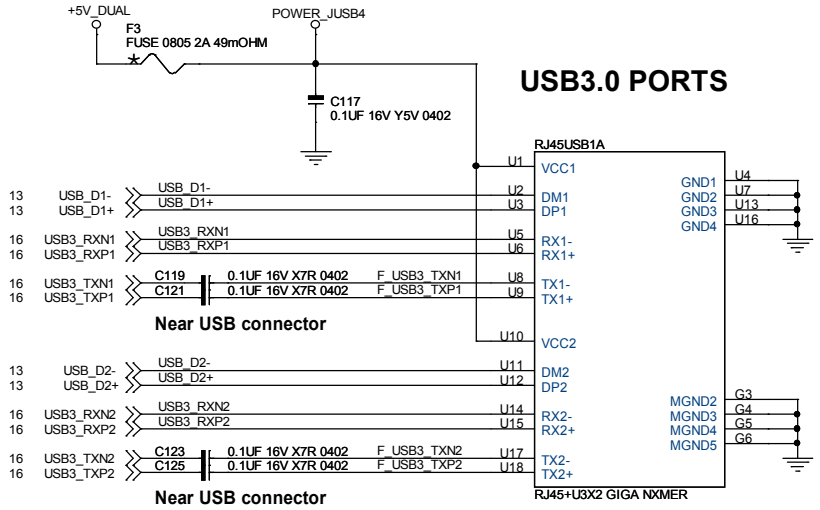

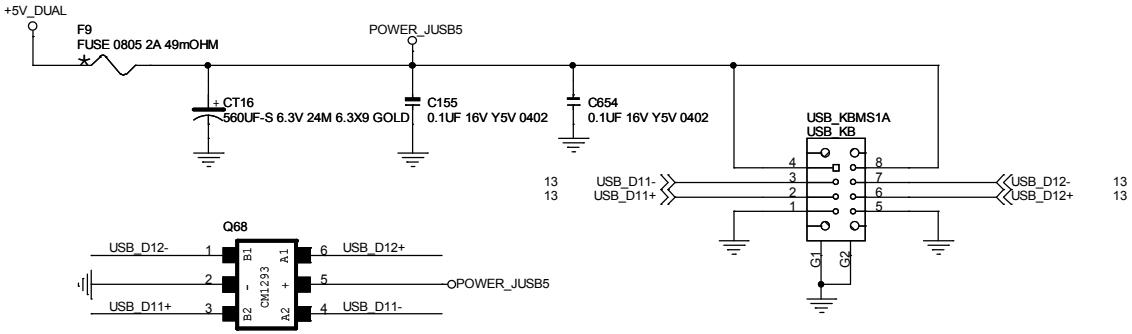

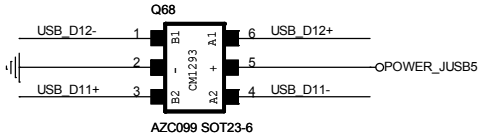

◇[illegible] INFORMATION◆

◇<[illegible] duplication, or disclosure of this document will be subject to the applicable civil and/orcriminal penalties.◆

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BIOSTAR GROUP

Title	REAR USB	
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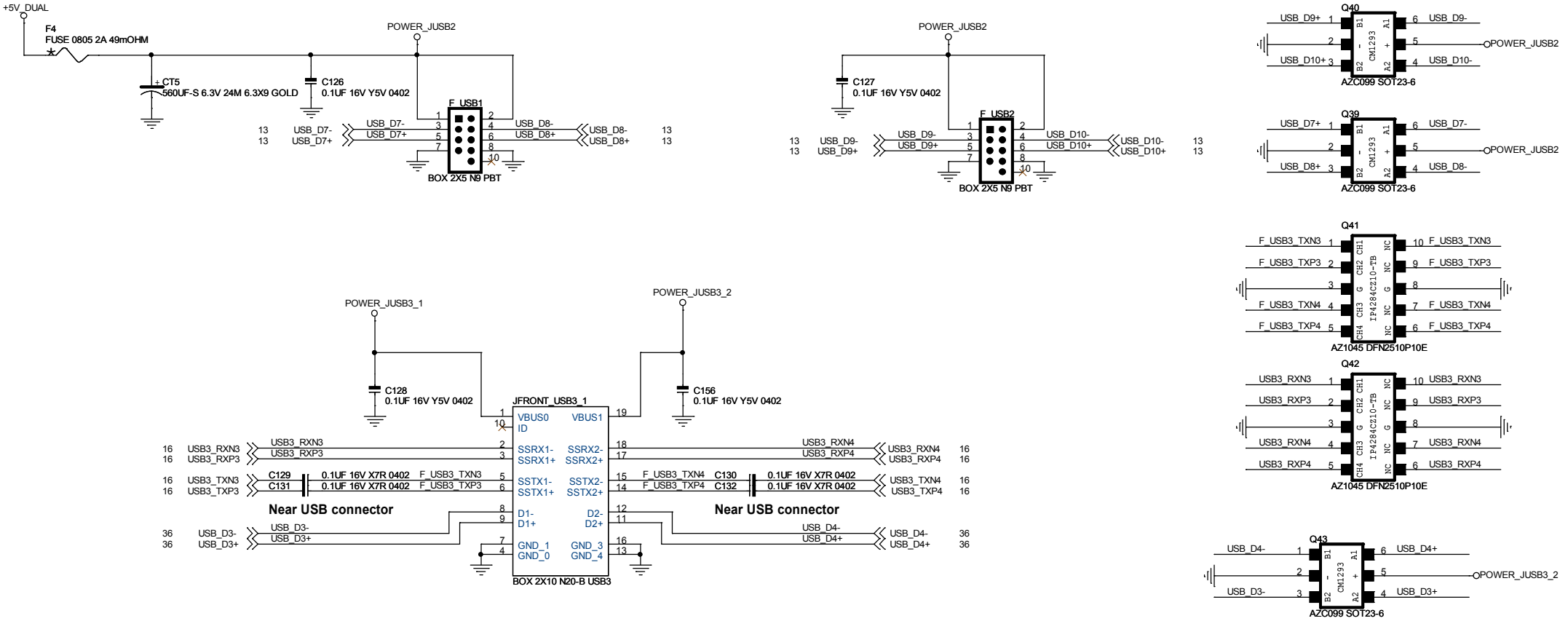

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Title	FRONT USB	
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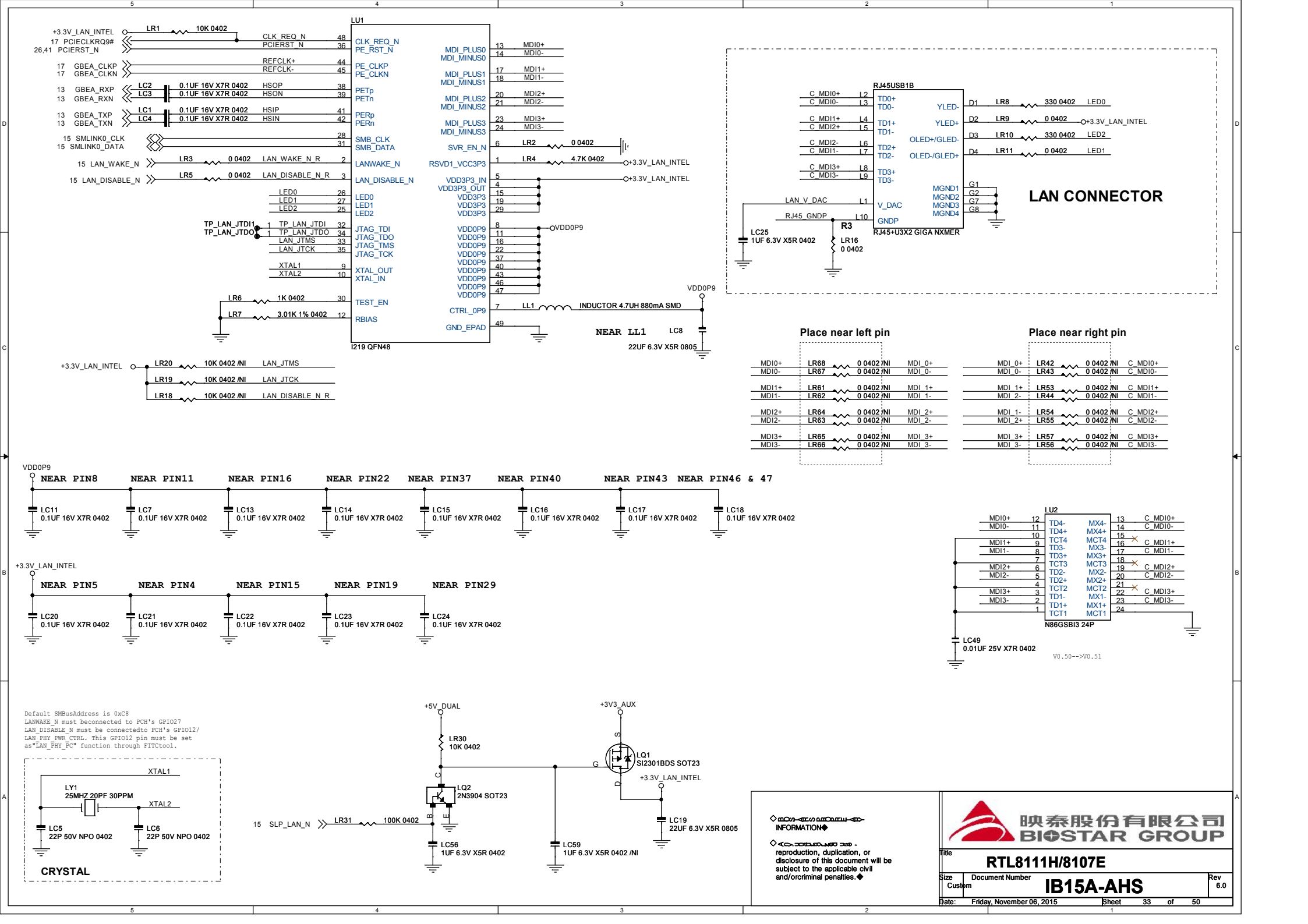
BC_USB_D4- 13,36
BC_USB_D4+ 13,36


LU1
I219 QFN48
LAN CONNECTOR
RJ45USB1B
RJ45+U3X2 GIGA NXMER
Place near left pin
Place near right pin
NEAR PIN8
NEAR PIN11
NEAR PIN16
NEAR PIN22
NEAR PIN37
NEAR PIN40
NEAR PIN43
NEAR PIN46 & 47
NEAR PIN5
NEAR PIN4
NEAR PIN15
NEAR PIN19
NEAR PIN29
NEAR LL1
LU2
N86GSBI3 24P
CRYSTAL
LY1
25MHZ 20PF 30PPM
LQ1
SI2301BDS SOT23
LQ2
2N3904 SOT23
Default SMBusAddress is 0xC8
LANWAKE_N must beconnected to PCH's GPIO27
LAN_DISABLE_N must be connectedto PCH's GPIO12/
LAN_PHY_PWR_CTRL. This GPIO12 pin must be set
as"LAN_PHY_PC" function through FITCtool.
INFORMATION
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disclosure of this document will be
subject to the applicable civil
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BIOSTAR GROUP
RTL8111H/8107E
IB15A-AHS
Custom
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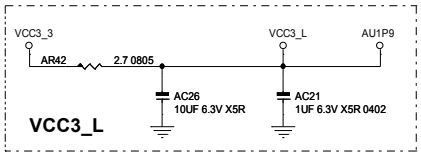
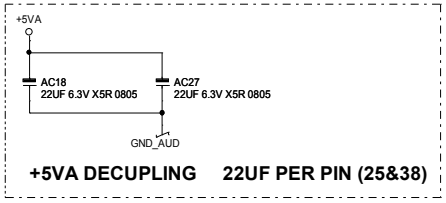
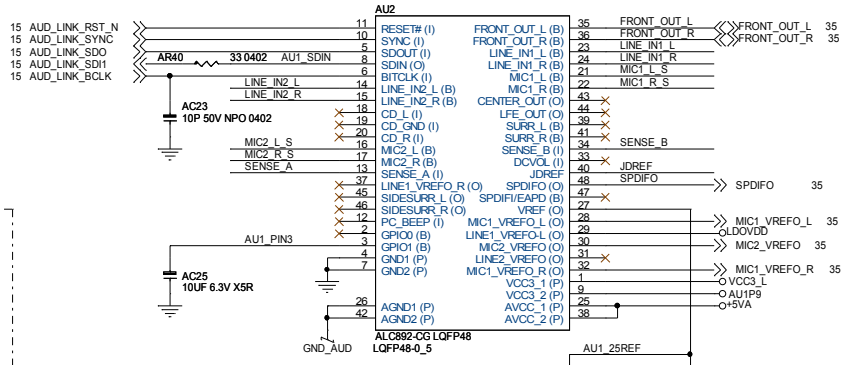
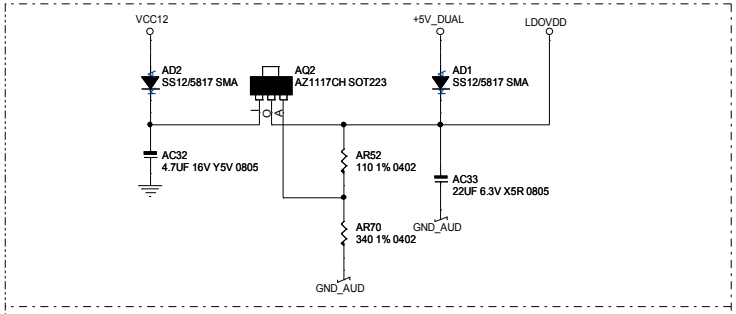
V0.50-->V0.51

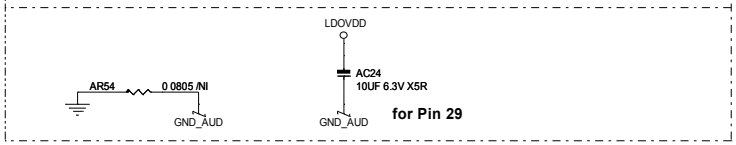
AUDIO PART: A+Reference

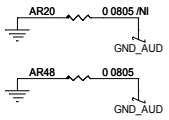


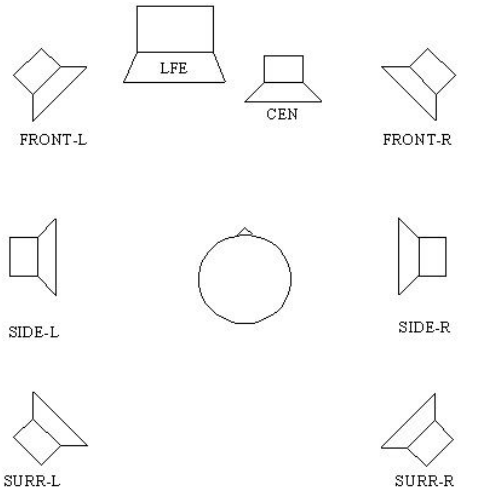




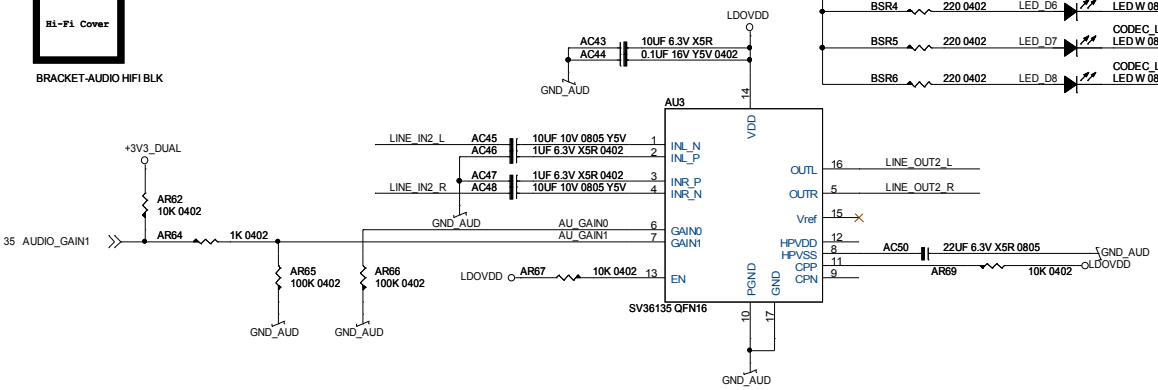


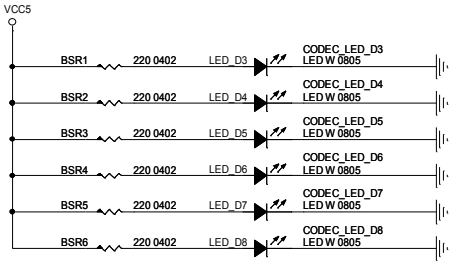


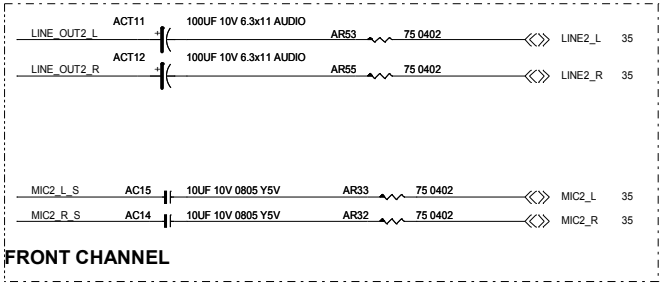


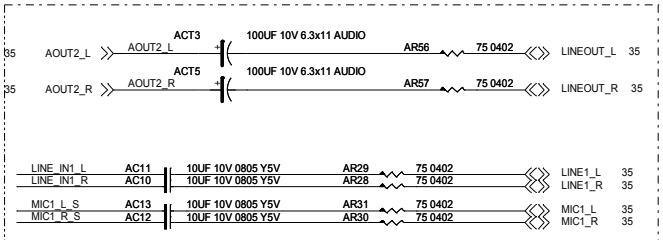


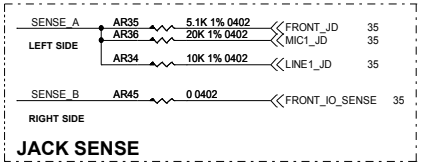
7.1SPEAKER CONFIGURATION

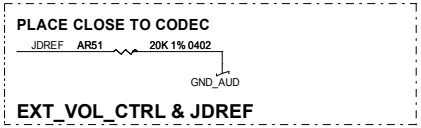


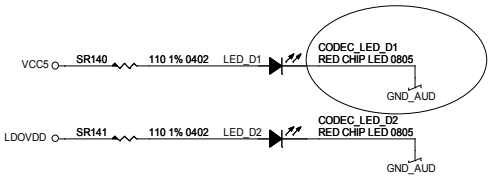












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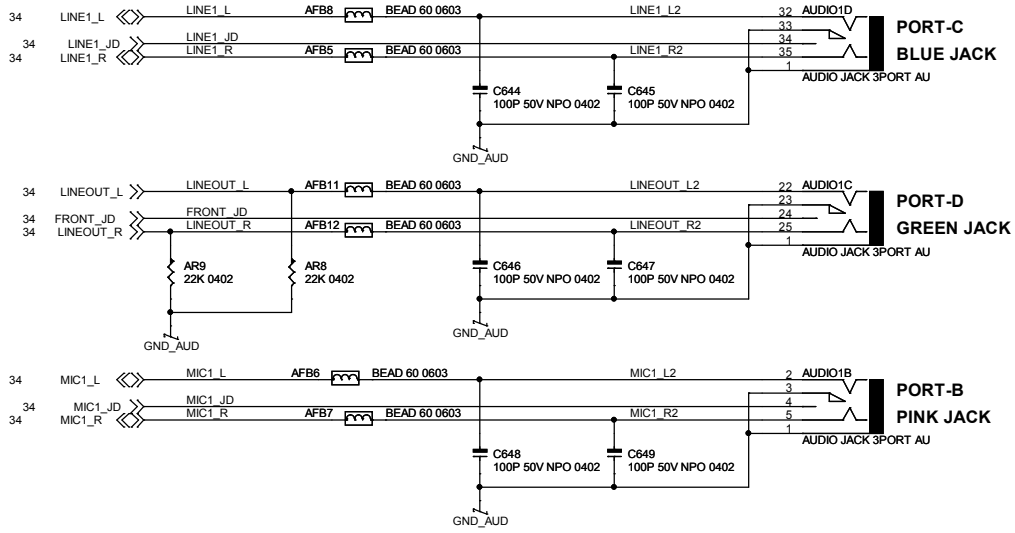
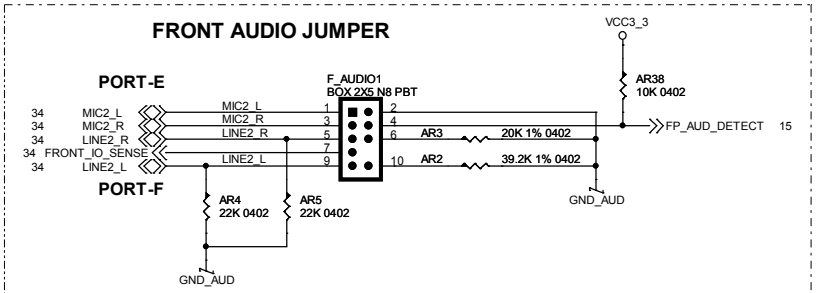
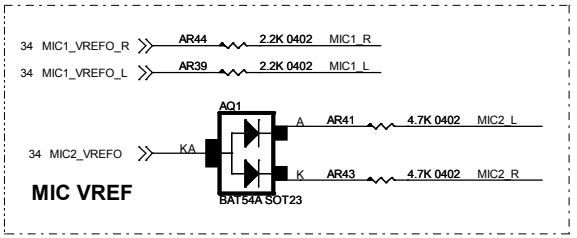
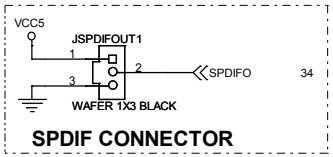
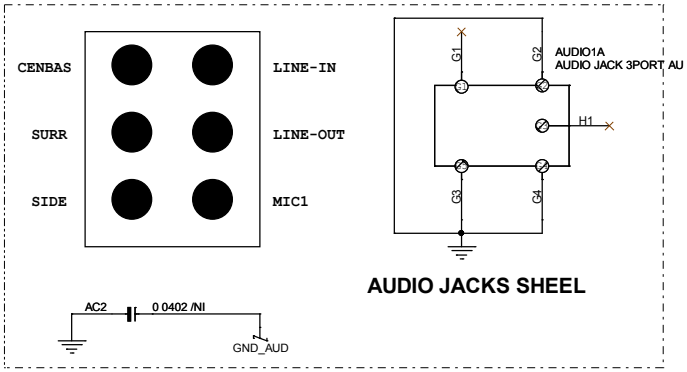








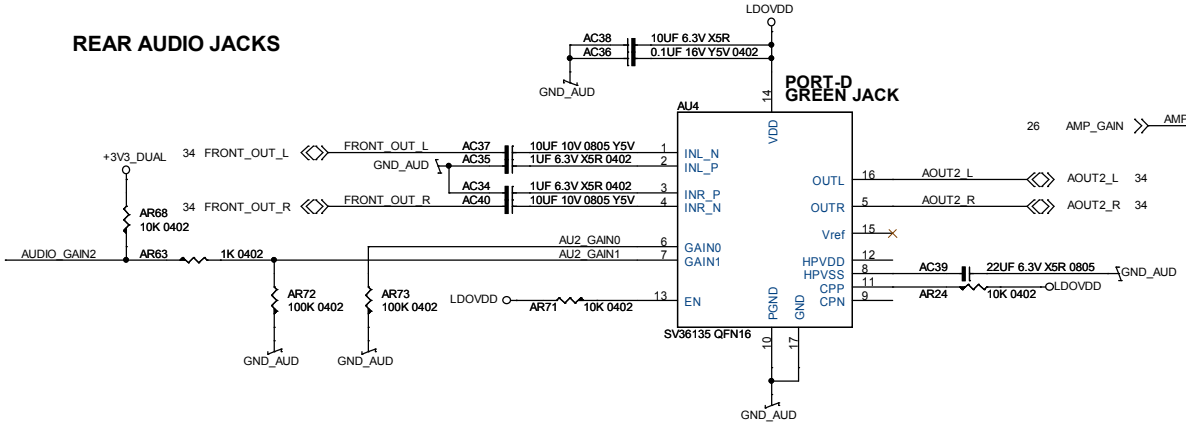
PORT-G
YELLOW JACK

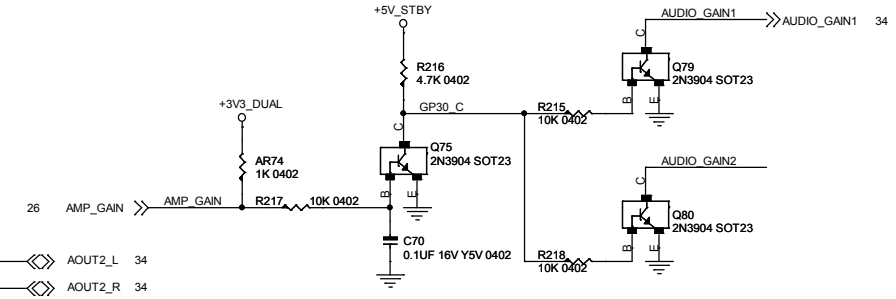


PORT-A
BLACK JACK

PORT-H
GRAY JACK

REAR AUDIO JACKS





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BIOSTAR GROUP

Title: AUDIO CONNECTOR

Size: Custom | Document Number: IB15A-AHS | Rev: 6.0

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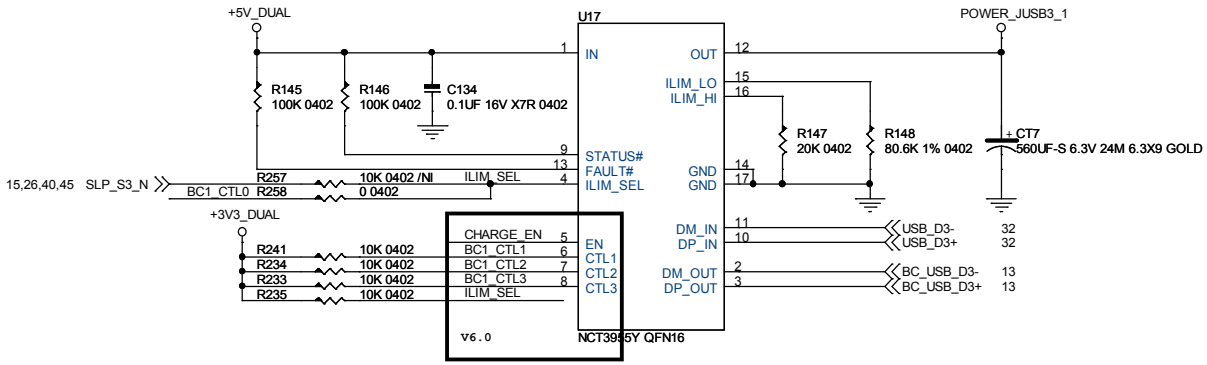

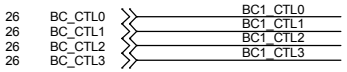

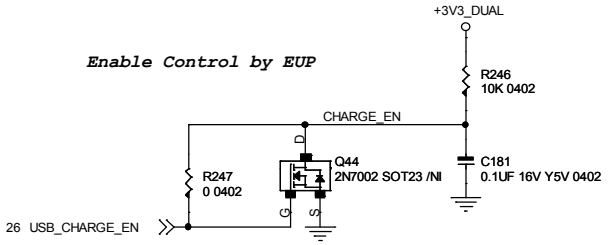

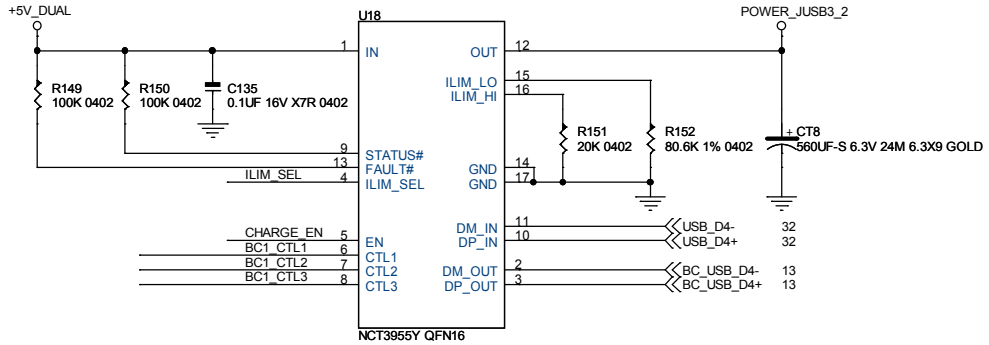

CTL1	CTL2	CTL3	ILIM_SEL	Mode	Current Limit Setting	STATUS# Output (Active Low)	Comment
1	1	1	0 (S3/S5)	SDP	ILM_LO	OFF	
1	1	1	1 (S0)	CDP	ILM_HI	CDP load present	Data Lines Connected and Port Power Mgt. Function Active

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Title: Charging uP7551

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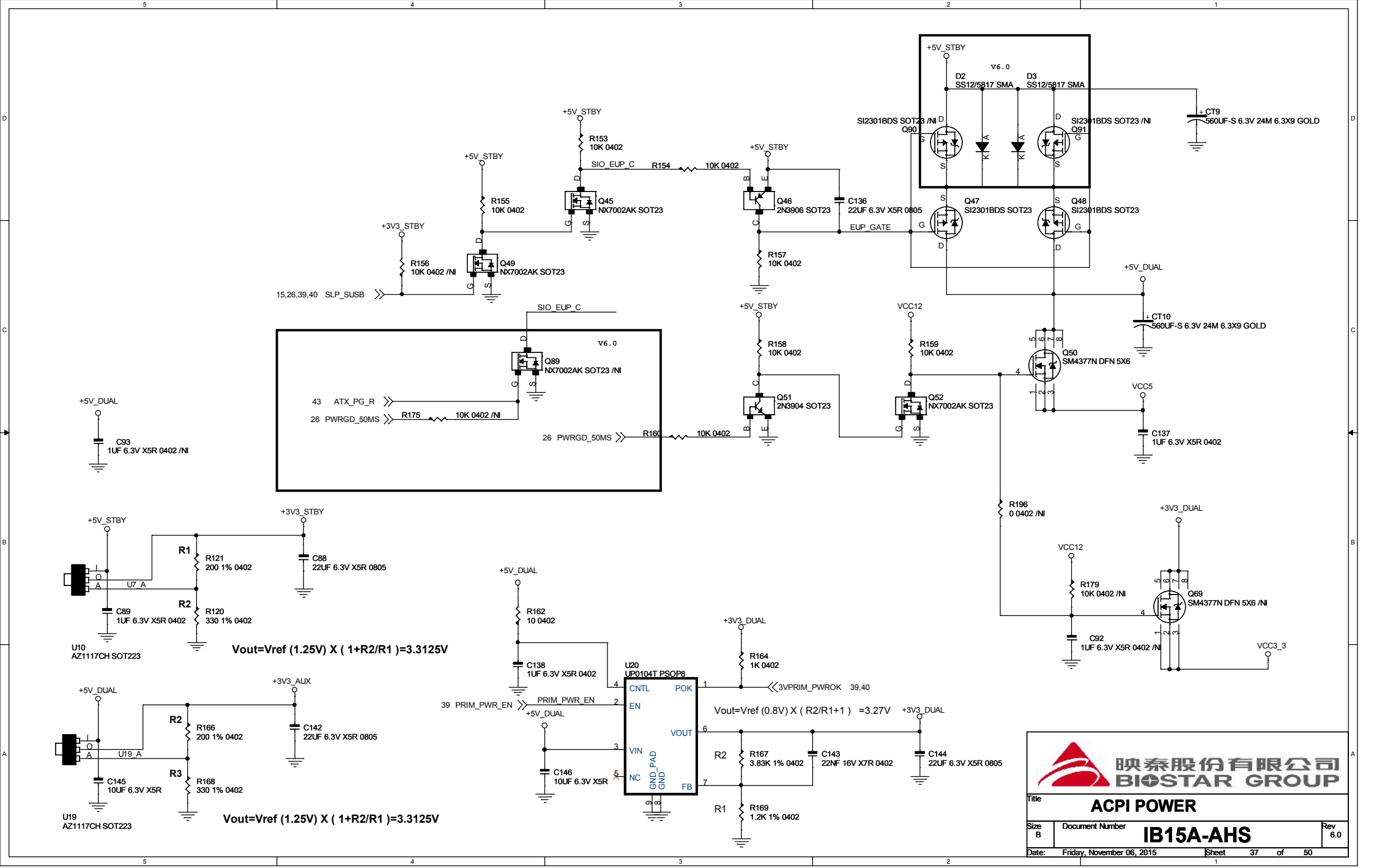
+5V_STBY
V6.0
D2
SS12/5817 SMA
D3
SS12/5817 SMA
SI2301BDS SOT23 /NI
Q90
SI2301BDS SOT23 /NI
Q91
CT9
560UF-S 6.3V 24M 6.3X9 GOLD
R153
10K 0402
SIO_EUP_C
R154
10K 0402
R155
10K 0402
Q45
NX7002AK SOT23
Q46
2N3906 SOT23
C136
22UF 6.3V X5R 0805
Q47
SI2301BDS SOT23
Q48
SI2301BDS SOT23
+3V3_STBY
R156
10K 0402 /NI
Q49
NX7002AK SOT23
15,26,39,40 SLP_SUSB
EUP_GATE
R157
10K 0402
+5V_DUAL
CT10
560UF-S 6.3V 24M 6.3X9 GOLD
SIO_EUP_C
Q89
NX7002AK SOT23 /NI
43 ATX_PG_R
26 PWRGD_50MS
R175
10K 0402 /NI
R158
10K 0402
R159
10K 0402
VCC12
Q50
SM4377N DFN 5X6
Q51
2N3904 SOT23
Q52
NX7002AK SOT23
VCC5
C137
1UF 6.3V X5R 0402
+5V_DUAL
C93
1UF 6.3V X5R 0402 /NI
R196
0 0402 /NI
+5V_STBY
+3V3_STBY
R1
R121
200 1% 0402
C88
22UF 6.3V X5R 0805
U7_A
R2
C89
1UF 6.3V X5R 0402
R120
330 1% 0402
U10
AZ1117CH SOT223
Vout=Vref (1.25V) X (1+R2/R1)=3.3125V
+3V3_DUAL
VCC12
R179
10K 0402 /NI
Q69
SM4377N DFN 5X6 /NI
C92
1UF 6.3V X5R 0402 /NI
VCC3_3
+5V_DUAL
R162
10 0402
C138
1UF 6.3V X5R 0402
U20
UP0104T PSOP8
CNTL
POK
EN
VOUT
VIN
NC
GND_PAD
GND
FB
+3V3_DUAL
R164
1K 0402
3VPRIM_PWROK 39,40
39 PRIM_PWR_EN
PRIM_PWR_EN
Vout=Vref (0.8V) X (R2/R1+1) =3.27V
+3V3_DUAL
+5V_DUAL
C146
10UF 6.3V X5R
R2
R167
3.83K 1% 0402
C143
22NF 16V X7R 0402
C144
22UF 6.3V X5R 0805
R1
R169
1.2K 1% 0402
+5V_DUAL
+3V3_AUX
R2
R166
200 1% 0402
C142
22UF 6.3V X5R 0805
U19_A
R3
C145
10UF 6.3V X5R
R168
330 1% 0402
U19
AZ1117CH SOT223
Vout=Vref (1.25V) X (1+R2/R1)=3.3125V
映泰股份有限公司
BIOSTAR GROUP
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ACPI POWER
Size
B
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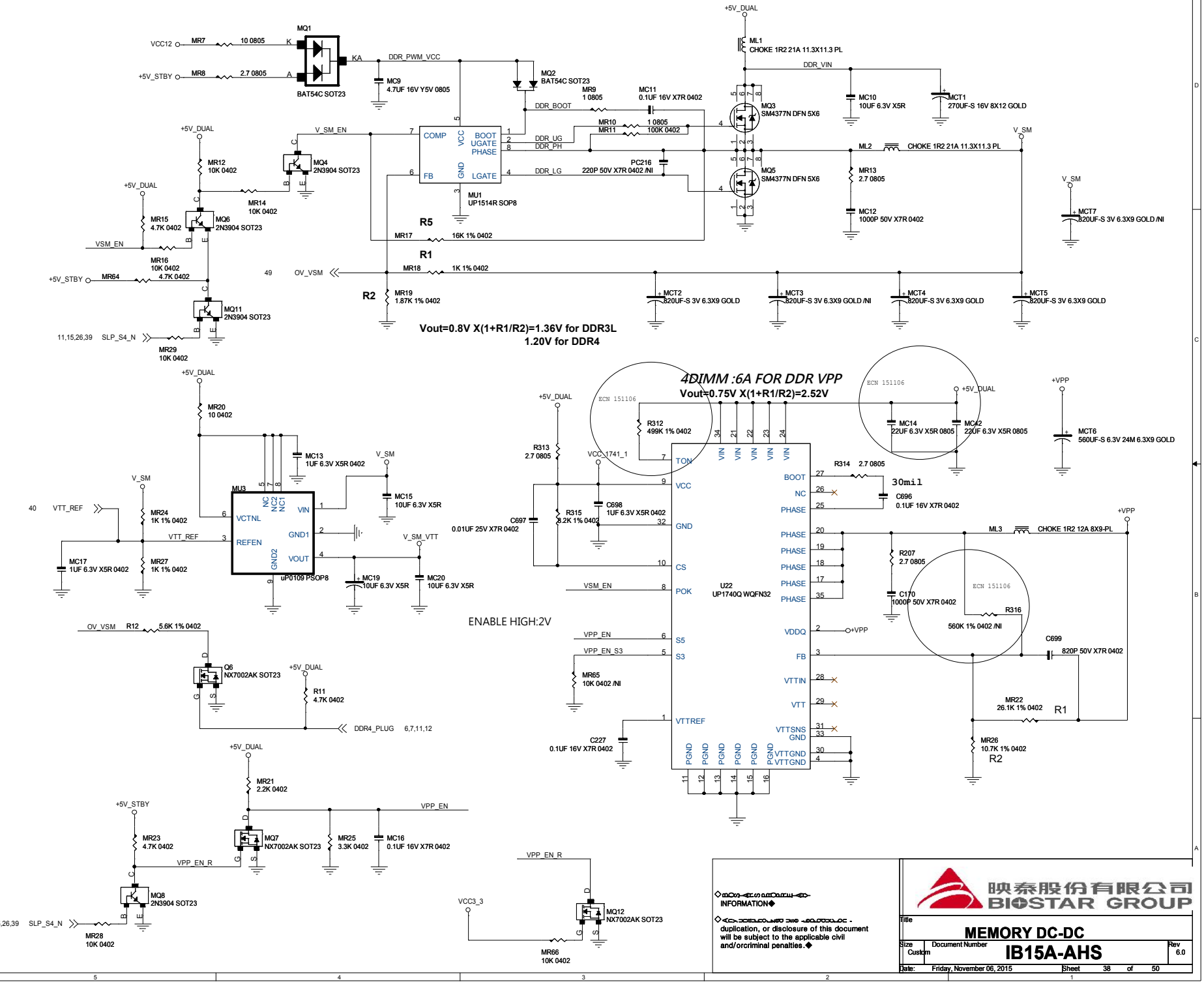
MEMORY PART:M+Reference



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BIOSTAR GROUP

Title	MEMORY DC-DC		
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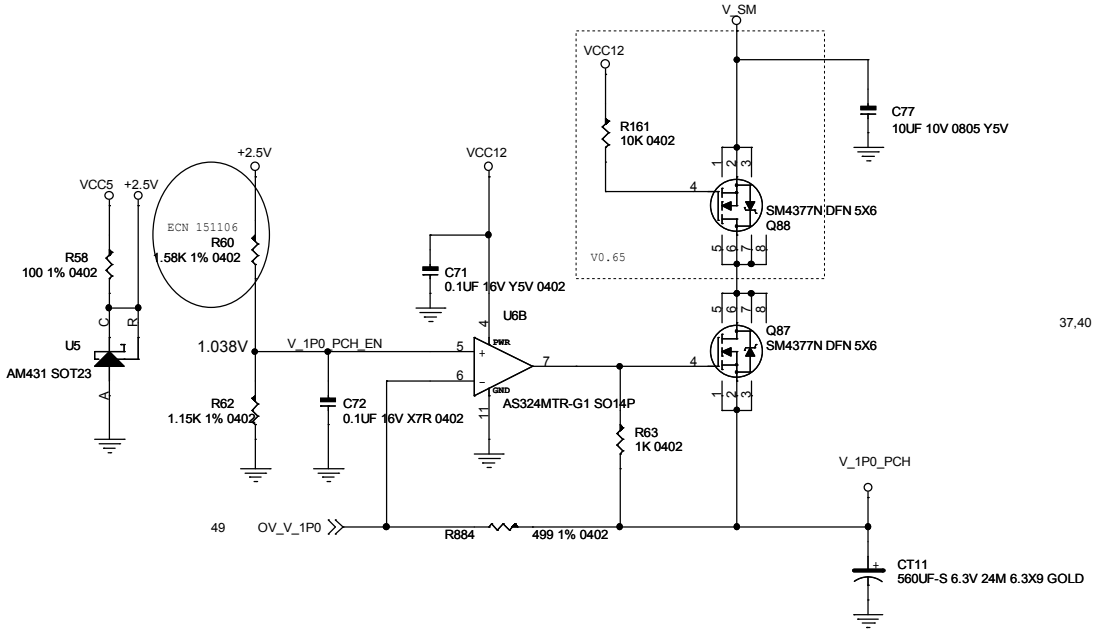
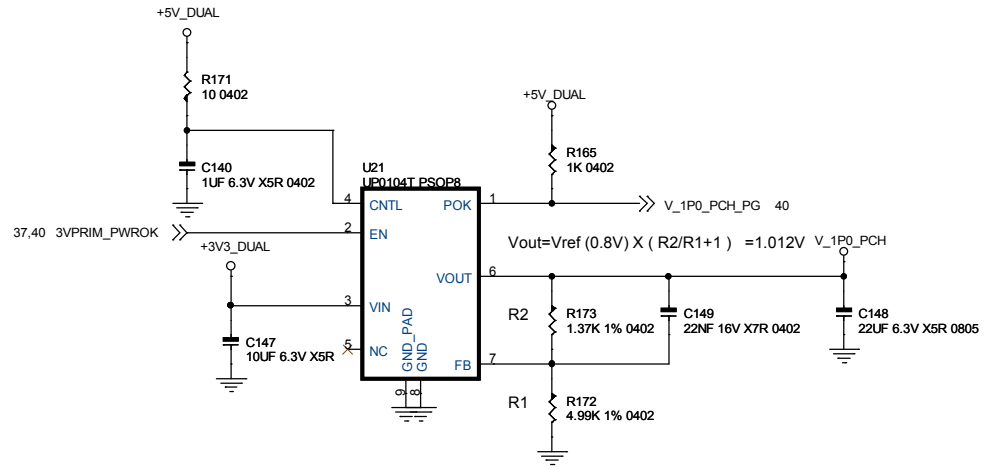
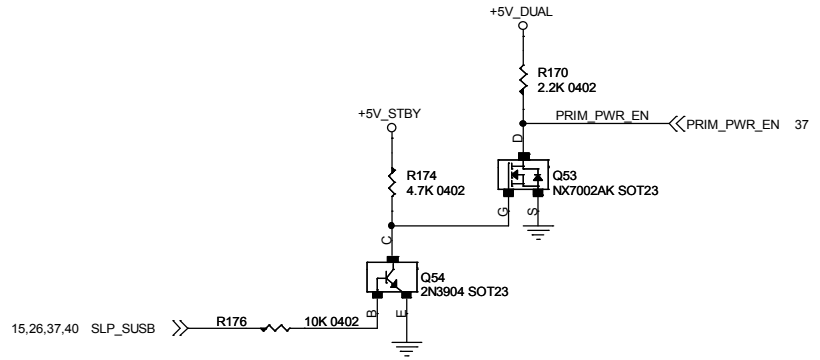
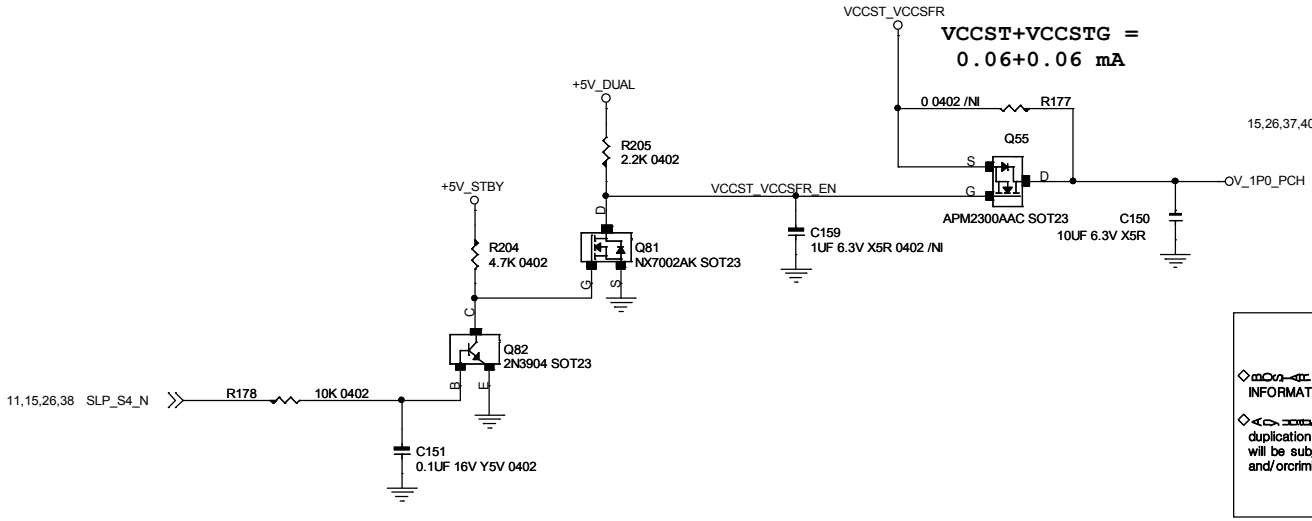
PCH Power:1.0V 7A

Vout=0.75V X(1+R1/R2)=1.03V









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Title	V_1P8 & V_1P0_PCH	
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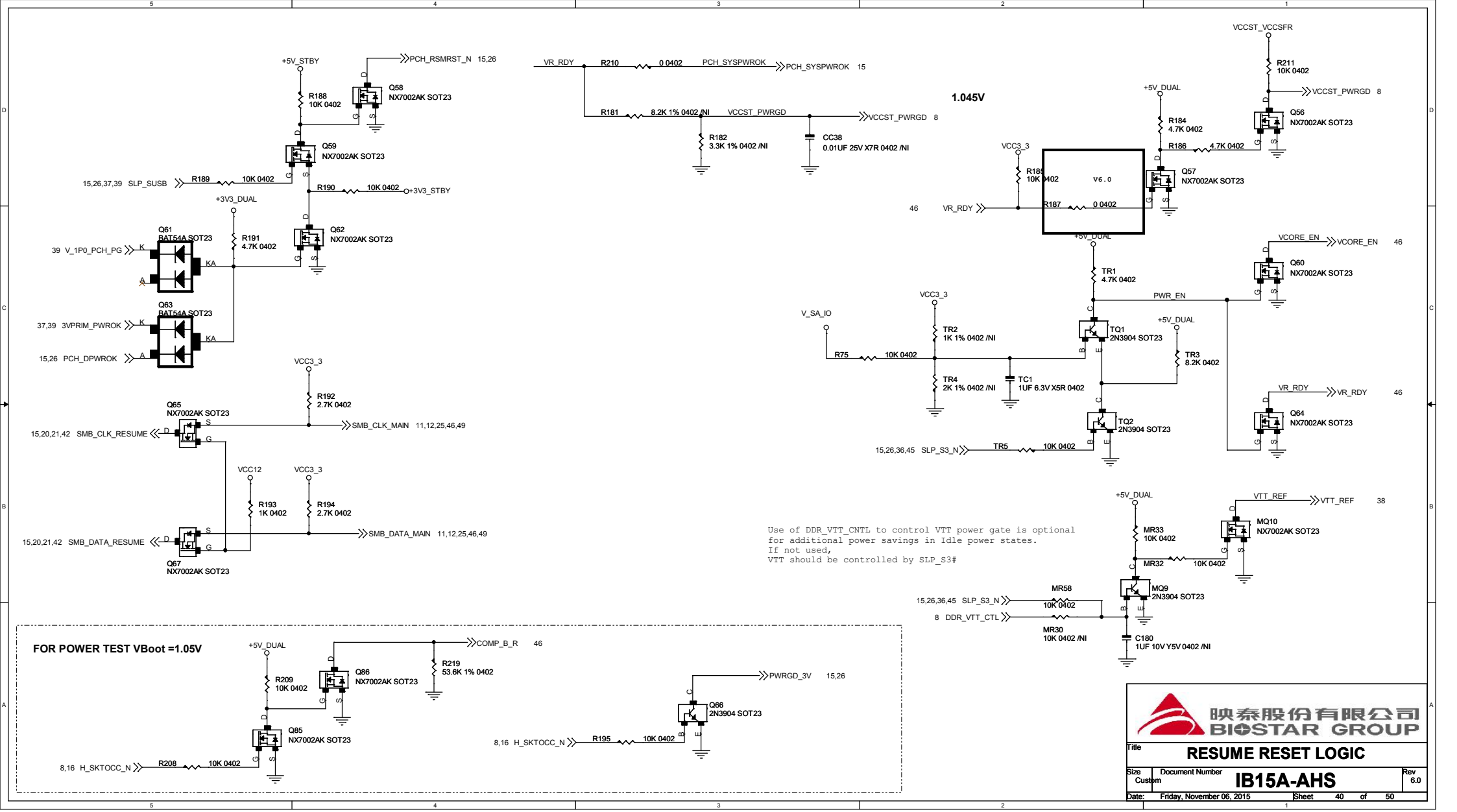

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Title: **RESUME RESET LOGIC**

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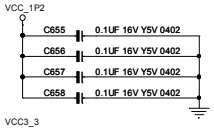
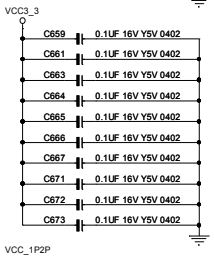
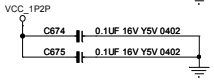
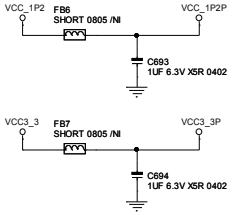
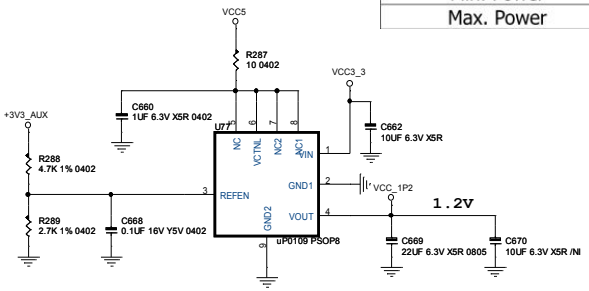
	3.3V	1.2V
Min. Power	70mA	100mA
Max. Power	90mA	115mA



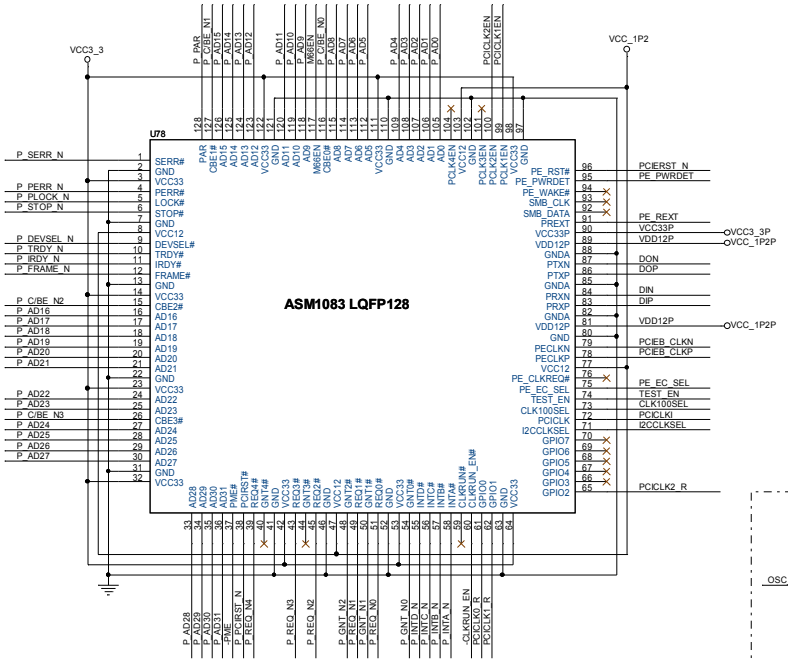


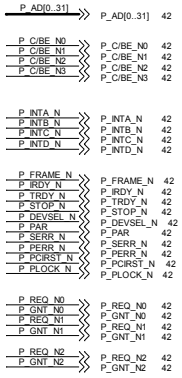


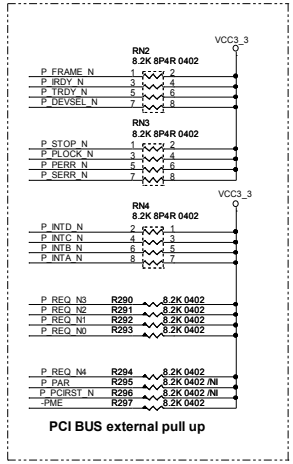


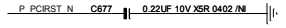


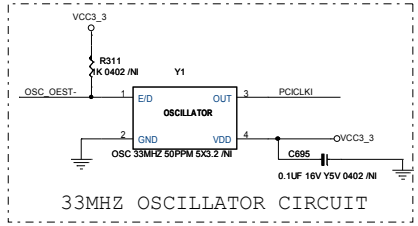
For ASM1083 Pin 101
and Pin 104 is NC Pin











CLK100SEL Strapping Set

CLK100SEL	H	L
PCIe CLK	100M +/-N%	100M +/-N%
PCICLK_IN	X	33M
PCICLKO	33M +/-N%	33M

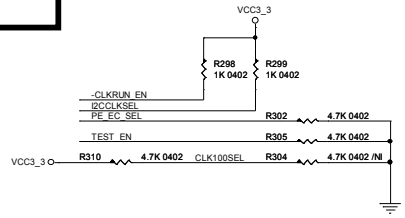
PE_EC_SEL-
"H" for Express Card mode
"L" for PCIe Riser Card mode

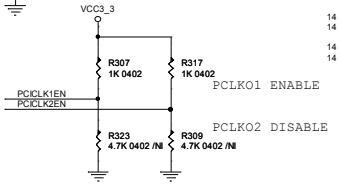
CLK100SEL-
"H" for PECLK input only
"L" for PECLK & PCICLK input

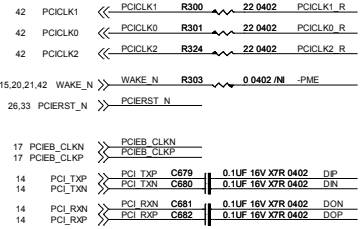
TEST_EN-
"H" for Test Mode Enable
"L" for Test Mode Disable

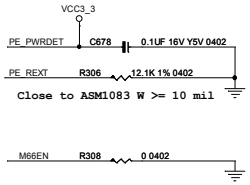
-CLKRUN_EN-
"H" for CLKRUN Mode Disable
"L" for CLKRUN Mode Enable

I2CCLKSEL-
"H" is 135KHz I2CCLK
"L" is 67.5KHz I2CCLK









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Title: PCI BRIDGE ASM1083

Size: C | Document Number: IB15A-AHS | Rev: 6.0

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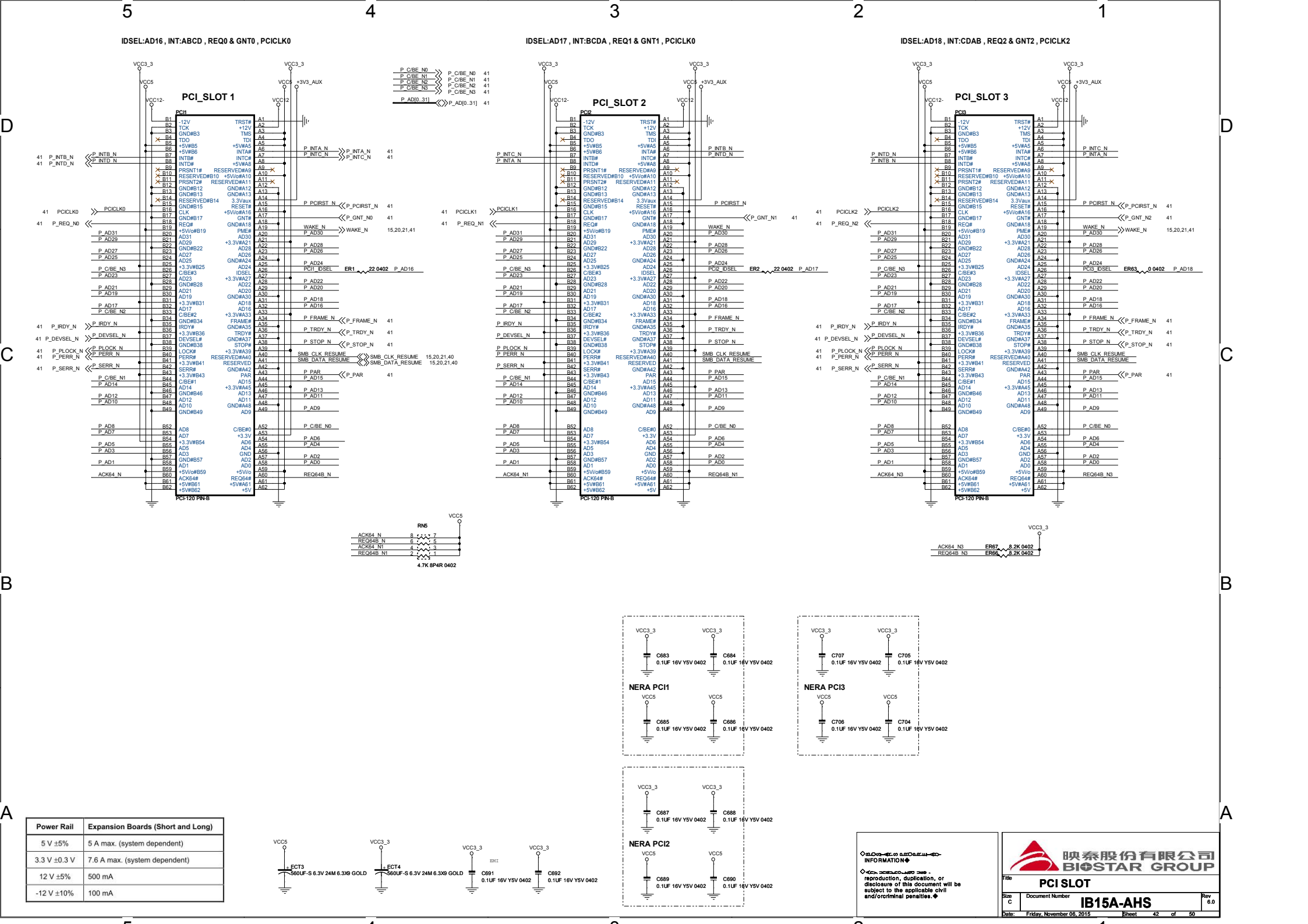

Power Rail	Expansion Boards (Short and Long)
5 V ±5%	5 A max. (system dependent)
3.3 V ±0.3 V	7.6 A max. (system dependent)
12 V ±5%	500 mA
-12 V ±10%	100 mA

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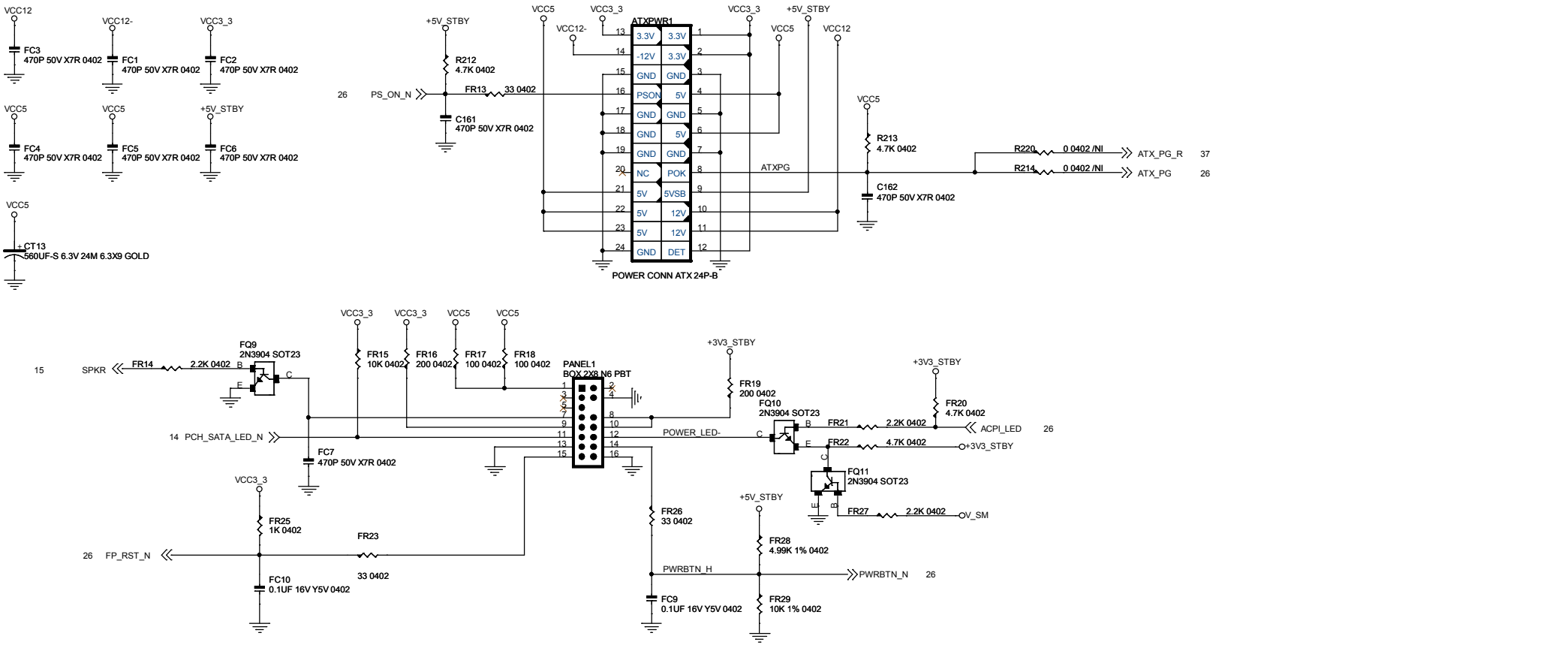
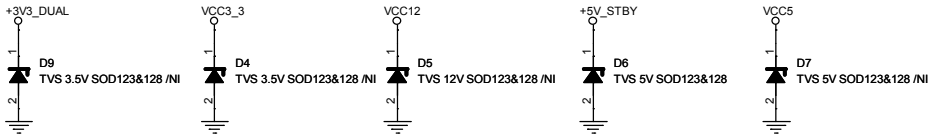
Title: PCI SLOT

Size: C | Document Number: IB15A-AHS | Rev: 6.0

Date: Friday, November 06, 2015 | Sheet 42 of 50

FP PART: F+Reference





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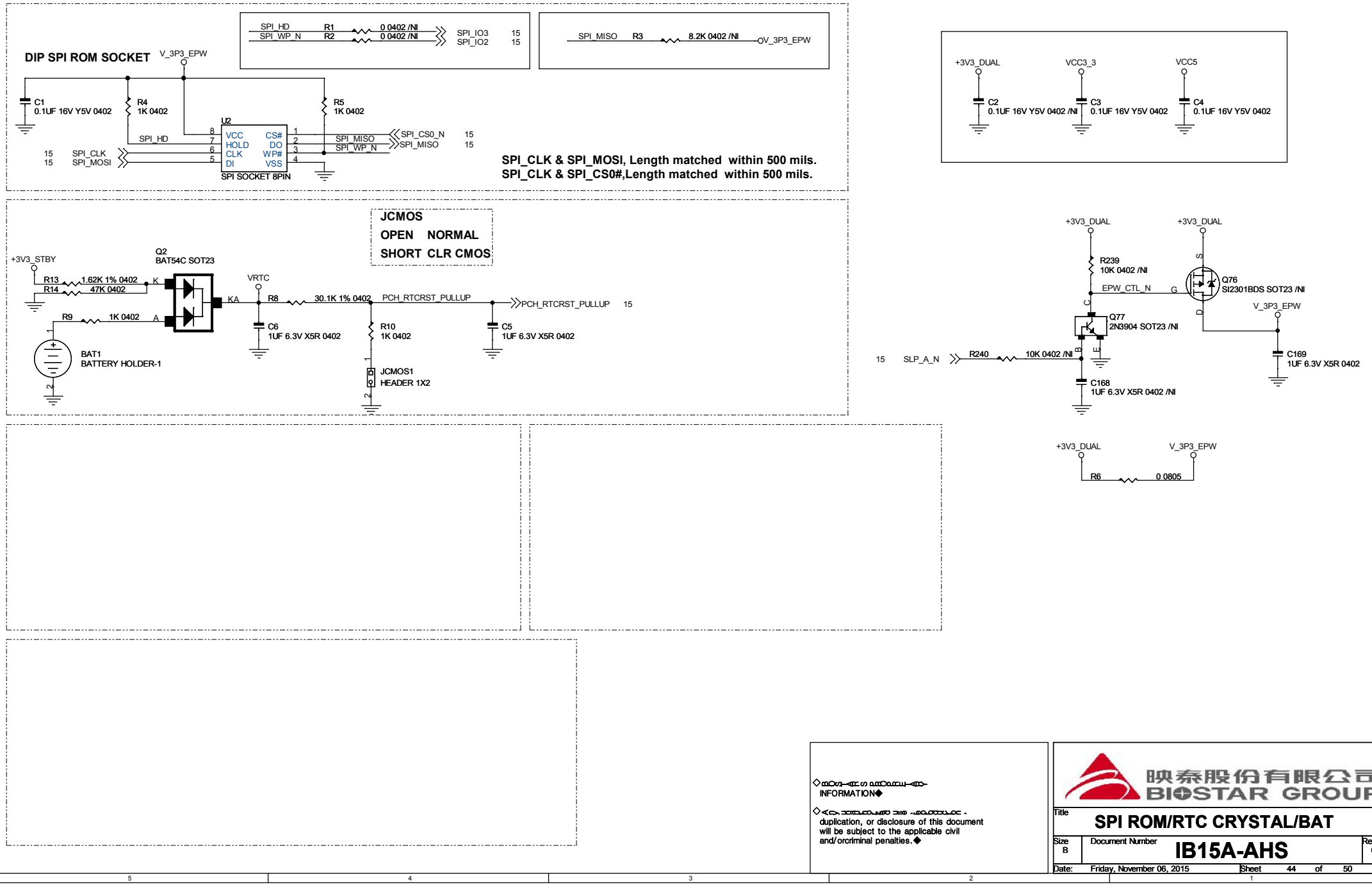
Title	24PIN CONN & FP	
Size: Custom	Document Number: IB15A-AHS	Rev: 6.0
Date: Friday, November 06, 2015	Sheet 43 of 50	



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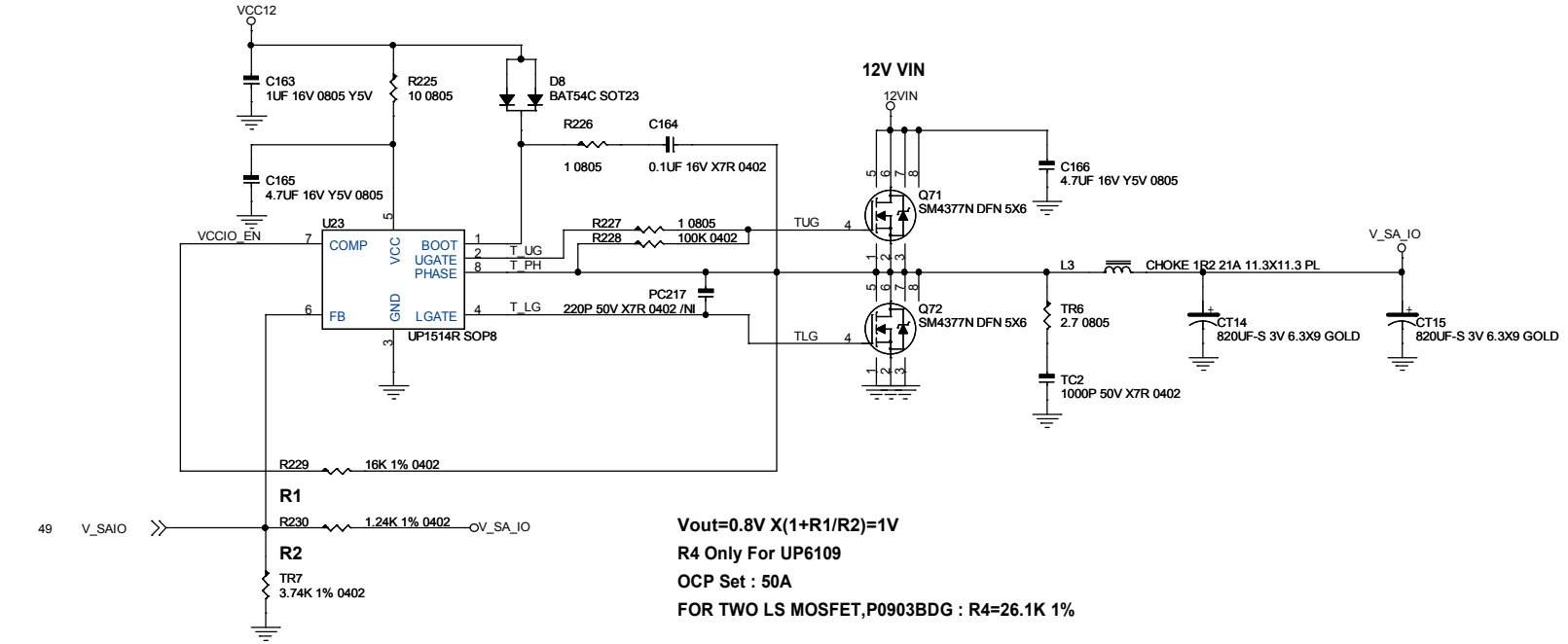
Title	SPI ROM/RTC CRYSTAL/BAT	
Size B	Document Number IB15A-AHS	Rev 6.0
Date: Friday, November 06, 2015	Sheet 44 of 50	

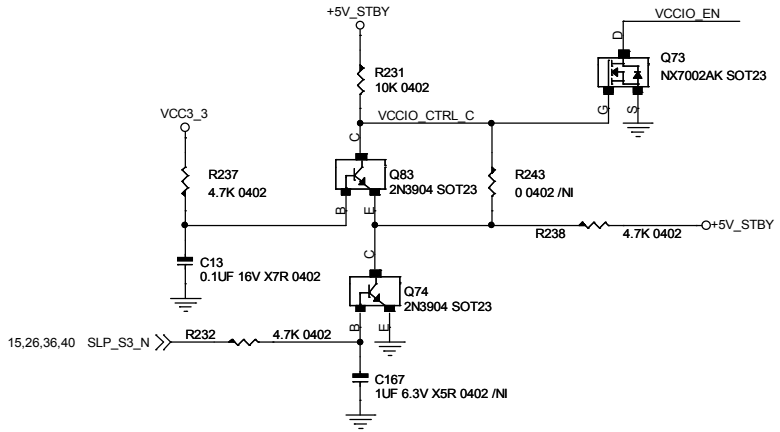


Vout=0.8V X(1+R1/R2)=1V

R4 Only For UP6109

OCP Set : 50A

FOR TWO LS MOSFET,P0903BDG : R4=26.1K 1%



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Title	24PIN CONN & FP	
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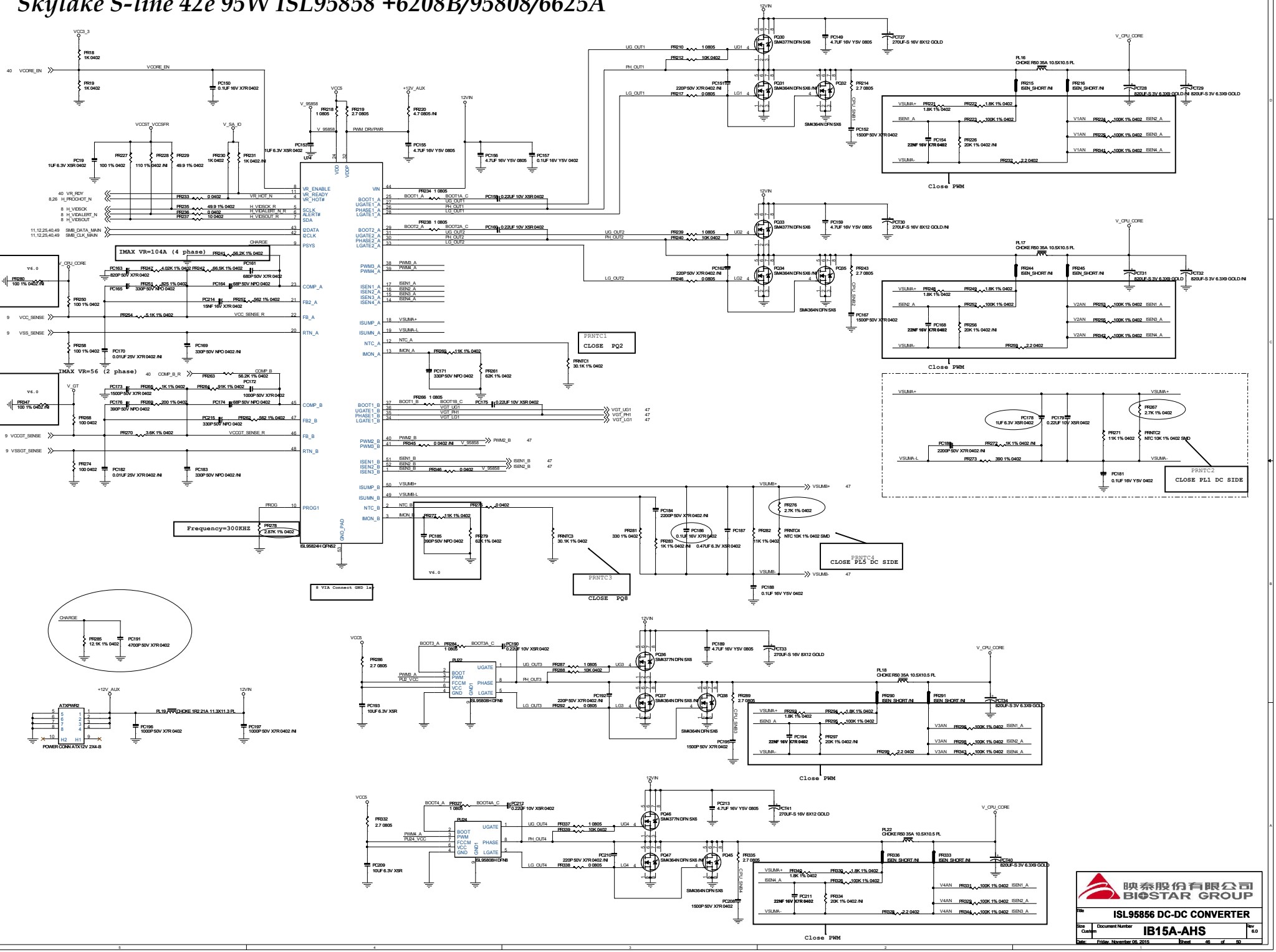
Skylake S-line 42e 95W ISL95858 +6208B/95808/6625A



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Title: ISL95856 DC-DC CONVERTER

Size: Custom | Document Number: IB15A-AHS | Rev: 6.0

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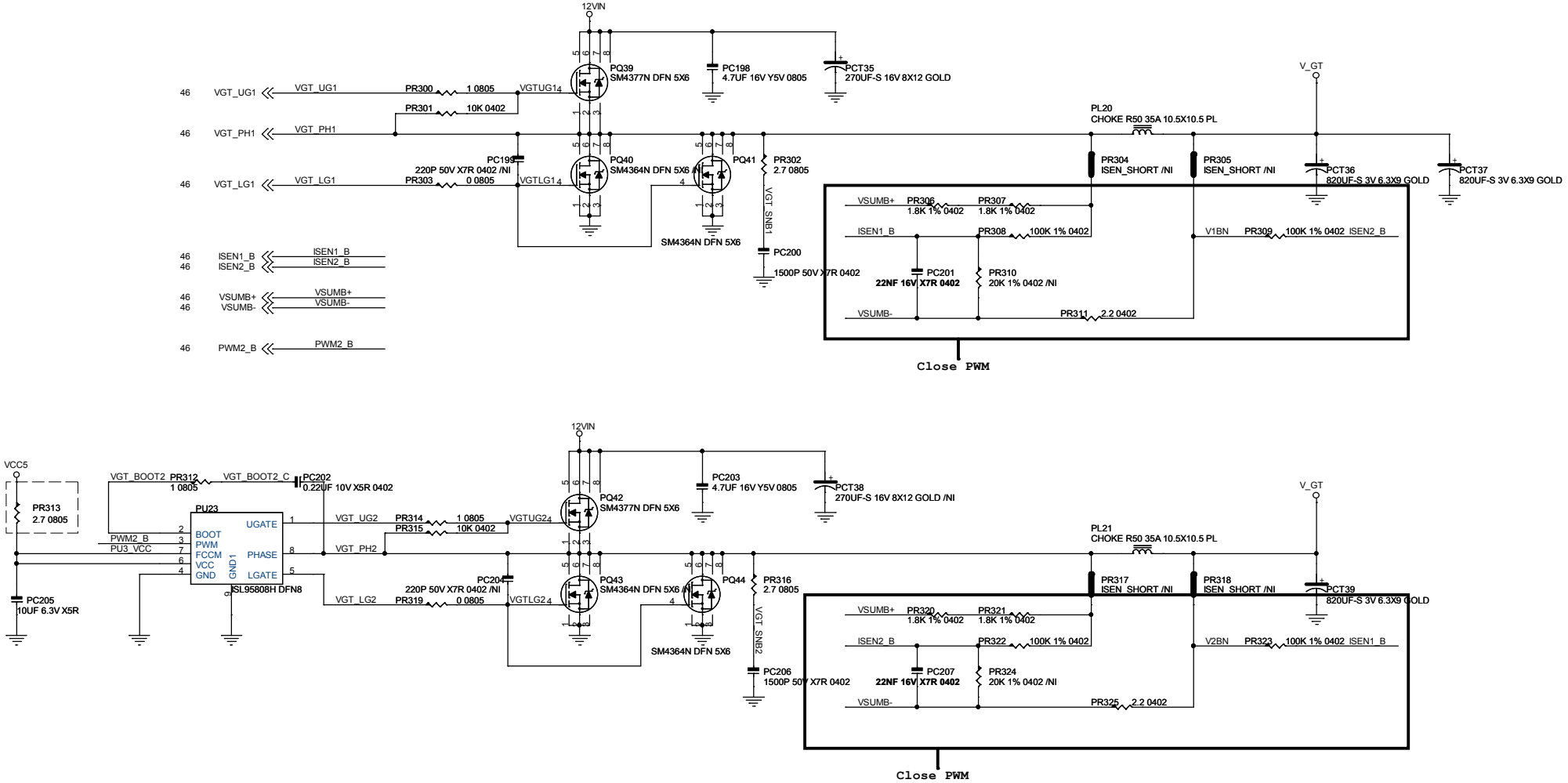
Skylake S-line 42 95W ISL95858_VGT



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Title	ISL95858 VGT PHASE	
Size: Custom	Document Number: IB15A-AHS	Rev: 6.0
Date: Friday, November 06, 2015	Sheet 47 of 50	

Skylake S-line 42 95W ISL95857 VSA

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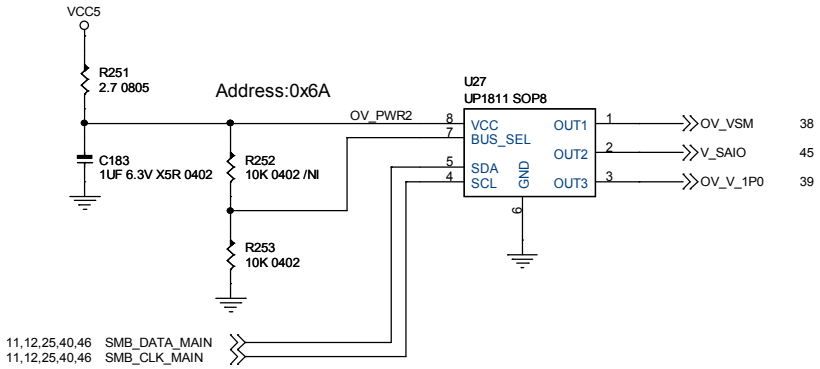
Title: CPU POWER

Size	Document Number	Rev
C	IB15A-AHS	6.0

Date: Friday, November 06, 2015 Sheet 48 of 50



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Title	OVER VOLTAGE	
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MH1
PAD200-8 /NI

MH2
PAD200-8 /NI
GND_AUD GND_AUD

MH5
PAD200-8 /NI

MH6
PAD200-8 /NI

MH9
PAD200-8 /NI

MH4
PAD200-8 /NI

MH7
PAD200-8 /NI
GND_AUD GND_AUD

MH3
PAD200-8 /NI

MH8
PAD200-8 /NI

MH10
PAD200-8 /NI

Impedance Testing Coupon

NC1 — TUNE2 (CP1, CP2) — HEADER 1X2 D 150 /NI

VCC12, NC2 — TUNE1 (CP1, CP2) — HEADER 1X2 D 150 /NI

New PANEL1

PANEL1 2*8

PANEL1(9_10) HEADER 1X2 /NI
PANEL1(15_16) HEADER 1X2 /NI
PANEL1(11_14) PLED /NI
PANEL1(1_4) SPK /NI
PANEL1(5_6) HLED /NI
PANEL1(7_8) RST /NI

(U2) FLASH ROM — SPI W25Q64 DIP

JCMOS1(1_2) JUMPER 2P B /NI

DDR_SEL(1_2) JUMPER 2P B /NI

(BAT1) 電池 — 3V BATTERY SONY

(CPU1) — LGA 1156 FRAME

PCB — IZ17A-AHS V6.0

(YY2) — X'TAL WIRE

(MOS1) — MOSHS-AA68AA2S

(MOS2) — MOSHS-AA68AA2S

(PCH1) — SBHS-IH17B

(LB2) LABEL — VER7.4 10X3 LB2 /NI

(LB1) LABEL — L-HI-FI B150Z5

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Title	BOM	
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